The One Card That Gets It All Together

PerCom's CI-812

With just one card, you can interface your S-100 bus computer to a data terminal and cassettes, and you can choose the data rates: 30, 60, 120, or 240 self-clocking bytes per second cassette interfacing, and 300- to 9600-baud data terminal interfacing.

The CI-812 not only combines both functions on one card, it also out-performs the separate interface cards normally required for cassette/terminal interfacing. The result: you pay less for more.

Available from

- The CI-812 provides the two most commonly required functions on one PC board: cassette interfacing and data terminal interfacing.
- The CI-812 provides selectable data rates: 30, 60, 120, or 240 KC /biphase-encoded bytes per second for cassette interfacing, and 300- to 9600-baud RS-232 interfacing.
- The CI-812 is designed with phase-locked /UART data recovery circuitry for extremely dependable, self-clocking data recovery, even with inexpensive audio cassette recorders.
- The CI-812's independent record-playback circuits accommodate two recorders for simultaneous operations such as cross-filing. Further, program control of recorders is available with an optional DIP reed relay kit.
- User software modification is minimal, if needed at all.
- A comprehensive instruction /application manual, with software, is included with each unit.

PERCOM

over

SPECIFICATIONS: CI-812

ENCODING METHOD

'Kansas City' (BYTE) - Biphase standard: Serial start-stop asynchronous with two stop bits, non-saturating, self-clocking synchronous frequency shift. The encoding method is the Biphase-M, or Manchester Code, with varying amounts of redundancy. 300 baud uses 8 cycles of 2400-Hz signal to define a logic 'one' bit, and 4 cycles of 1200-Hz signal for a logic 'zero'. At 2400 baud, a logic 'one' is one cycle of 2400-Hz signal and a 'zero' is one half cycle of 1200 Hz.

DATA RATE (cassette)

Selectable: 300, 600, 1200 or 2400 baud. 300 baud is 'Kansas City Standard' rate. Cassette data rate is independent of Data Terminal rate selection.

ERROR RATE

Typically less than one error per million bytes at 300 baud using premium quality audio tape and well-maintained $50 - $100 cassette tape units. 2400-baud operation should be regarded as experimental although satisfactory performance will be obtained with moderate quality cassette recorders in non-critical applications.

STORAGE CAPACITY

A C-60 cassette will hold 96K bytes at 300 baud or 750K bytes at 2400 baud. Cassettes longer than C-60 are NOT recommended.

COMPUTER INTERFACE

Compatible electrically and physically with the Altair, IMSAI and other computers using the S-100 bus. The CI-812 is I/O driven with selectable I/O address. Control and status is I/O port xxxx xxx0; data is I/O port xxxx xxx1.

DATA TERMINAL INTERFACE

Full duplex, RS-232 levels at 300, 600, 1200, 2400, 4800, or 9600 baud. Selection of Cassette or Data Terminal input is under program control.

CASSETTE AUDIO INTERFACE

Compatible with the Earplug output and the AUX or MIC inputs on most portable cassette recorder/players.

POWER REQUIREMENTS

+8 Vdc ±1 Vdc @ 500 mA (provided by host computer)
−16 Vdc ±1 Vdc @ 20 mA (provided by host computer)

PHYSICAL

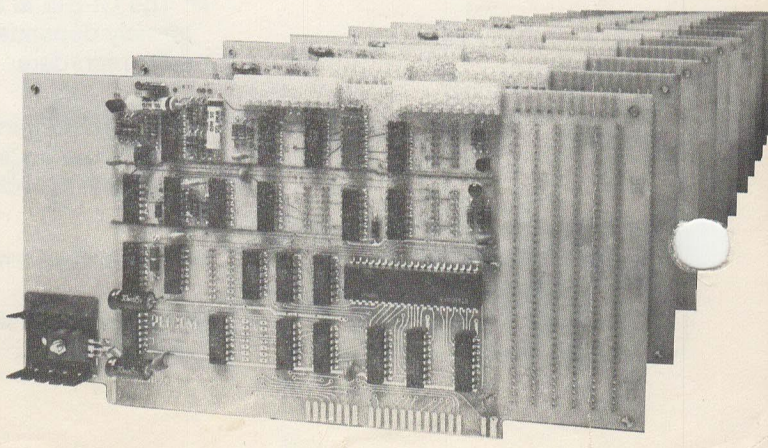
Altair/IMSAI/S-100 sized circuit card (10″ × 5.375″). PC card is FR4-G10 epoxy glass, double-sided, 2-oz copper, with plated-thru holes. Edge contacts are gold.

CI-812 (kit)	$89.95.
CI-812 (assembled)	$119.95.
I.C. Socket Kit*	$14.95.
Remote Control Kit	$10.95.
Test Cassette	$4.95.
Instruction Manual (price refunded with order)	$4.00.

*Use of IC sockets not supplied by PerCom will void warranty.

PERCOM

PERCOM DATA COMPANY, INC.
4021 WINDSOR • GARLAND, TEXAS 75042
(214) 276-1968



PerCom *'peripherals for personal computing'*

INTRODUCTION

THE PERCOM CI-812 IS THE ONLY INTERFACE YOU NEED TO COMPLETE YOUR ALTAIR/IMSAI OR SIMILIAR COMPUTER USING THE S-1ØØ BUSS STANDARD. THE CI-812 OUT PERFORMS AND COMBINES THE FUNCTIONS NORMALLY REQUIRING TWO OR THREE MORE COSTLY INTERFACE CIRCUIT CARDS.

IN ADDITION TO THE 3ØØ TO 96ØØ BAUD FULL DUPLEX DATA TERMINAL INTERFACE, THE CI-812 CONTAINS THE MOST USEFUL, MOST RELIABLE AUDIO CASSETTE INTERFACE YOU CAN BUY. DATA MAY BE RECORDED AND PLAYED BACK ON ORDINARY UNMODIFIED CASSETTE RECORDER/PLAYERS AT 3Ø, 6Ø, 12Ø OR 24Ø BYTES/SECOND. 3Ø BYTES/SECOND IS THE 'KANSAS CITY' STANDARD FOR RELIABLE DATA INTERCHANGE; USE 12Ø OR 24Ø BYTES/SECOND TO QUICKLY LOAD YOUR MOST FREQUENTLY USED PROGRAMS.

THE CASSETTE INTERFACE IS COMPATIBLE WITH THE 'KANSAS CITY' OR BYTE STANDARD. THIS PARTICULAR TECHNIQUE FOR RECORDING DATA ON AUDIO CASSETTE RECORDERS WAS SELECTED BY A SYMPOSIUM HELD IN KANSAS CITY, MO. IN THE FALL OF 1975. THE STANDARD IS BASED ON THE EXPERIMENTAL WORK OF DON LANCASTER OF SYNERGETICS AND HAROLD MAUCH OF PERCOM DATA CO.

DATA IS RECORDED ON TAPE, BIT SERIAL WITH A START BIT PRECEDING 8 DATA BITS AND TWO OR MORE STOP BITS. THE LOGIC ONE (MARKING STATE) IS IDENTIFIED AS 8 CYCLES OF A 24ØØ HERTZ SIGNAL. THE LOGIC ZERO (SPACING STATE) IS 4 CYCLES OF 12ØØ HERTZ SIGNAL. THE RECOVERED DATA IS SELF CLOCKING, VIRTUALLY ELIMINATING ERRORS CAUSED BY TAPE SPEED VARIATIONS WHICH PLAGUE THE FSK CASSETTE INTERFACES SUCH AS SUDING AND MITS.

ALTHOUGH THE 3ØØ BIT/SECOND (BAUD) RATE WAS CHOSEN TO PROVIDE MAXIMUM RELIABILITY FOR INTERCHANGE OF DATA, THE 'KANSAS CITY' STANDARD IS A HIGHLY (8X) REDUNDANT FORM OF THE BIPHASE-M OR MANCHESTER CODE. A UNIQUE FEATURE OF THE PERCOM CASSETTE INTERFACE IS THE CAPABILITY TO OPERATE AT RATES UP TO 24ØØ BAUD BY CONTROLLING THIS REDUNDANCY. 24ØØ BAUD PERMITS A 4K PROGRAM TO BE LOADED IN LESS THAN 2Ø SECONDS. MOST RELIABLE OPERATION WILL BE OBTAINED AT 3ØØ, 6ØØ OR 12ØØ BAUD.

THIS APPLICATION NOTE CONTAINS INSTRUCTIONS FOR ASSEMBLY, FOR CONNECTION AND USE OF THE CI-812 CASSETTE/TERMINAL INTERFACE.

ASSEMBLY INSTRUCTIONS FOR THE PERCOM CI-812

READ ALL OF THE FOLLOWING INSTRUCTIONS CAREFULLY

BE SURE TO READ THE WARRANTY PARTICULARLY NOTING THE STATEMENTS REGARDING CORROSIVE SOLDER FLUX AND INTEGRATED CIRCUIT SOCKETS.

CHECK THE KIT PARTS AGAINST THE PARTS LIST.

BRUSH BOTH SIDES OF THE PC CARD VIGOROUSLY WITH A DISCARDED TOOTHBRUSH TO REMOVE ANY ETCH SLIVERS WHICH MAY CAUSE INVISIBLE SHORTS.

INSTALL THE COMPONENTS IN THE FOLLOWING ORDER. REFER TO FIGURE 1 FOR COMPONENT LOCATION AND ORIENTATION.

CHECK THE ERRATA SHEETS FOR CHANGES TO THE FOLLOWING PROCEDURE.

RESISTORS:

CHECK	RESISTOR	VALUE	COLOR CODE
( )	R1	47K ¼W	YL VI OR
( )	R2	1ØK	BR BK OR
( )	R3	1ØØK	BR BK YL
( )	R4	1ØK	BR BK OR
( )	R5	68K	BU GR OR
( )	R6	4.7K	YL VI RD
( )	R7	1ØØK	BR BK YL
( )	R8	1ØK	BR BK OR
( )	R9	1ØK	BR BK OR
( )	R1Ø	1ØØK	BR BK YL
( )	R11	1K	BR BK RD
( )	R12	18Ø	BR GY BR
( )	R13	82Ø	GY RD BR
( )	R14	1K	BR BK RD
( )	R15	~~47Ø~~ 100	~~YL VI BR~~ BR BL BR
( )	R16	4.7K	YL VI RD
( )	R17	47K	YL VI OR
( )	R18	18Ø	BR GY BR
( )	R19	1ØK	BR BK OR
( )	R2Ø	1ØK	BR BK OR
( )	R21	1ØØ	BR BK BR
( )	R22	4.7K	YL VI RD
( )	R23	1K	BR BK RD
( )	R24	——	NOT USED
( )	R25	1K	BR BK RD
( )	R26	27K	RD VI OR
( )	R27	1ØK	BR BK OR
( )	R28	1ØK	BR BK OR
( )	R29	2.7K	RD VI RD
( )	R3Ø	1ØK	BR BK OR

BK-BLACK	Ø
BR-BROWN	1
RD-RED	2
OR-ORANGE	3
YL-YELLOW	4
GR-GREEN	5
BU-BLUE	6
VI-VIOLET	7
GY-GRAY	8
WH-WHITE	9

CHECK	RESISTOR	VALUE	COLOR CODE
( )	R31	4.7K	YL VI RD
( )	R32	18Ø ½W	BR GY BR
( )	R33		NOT USED

DIODES:

( )	CR1	1N914	
( )	CR2	*	NOT USED
( )	CR3	*	NOT USED
( )	CR4	1N759A	
( )	CR5	1N914	

SOLDER AND CLIP ALL RESISTOR AND DIODE LEADS

CAPACITORS:

CHECK	CAPACITOR	VALUE	TYPE
( )	C1	Ø.Ø47UF	MYLAR
( )	C2	Ø.Ø1UF	DISC
( )	C3	15ØPF	MICA
( )	C4	Ø.Ø47UF	MYLAR
( )	C5	Ø.Ø1UF	DISC
( )	C6	75ØPF	DISC
( )	C7	Ø.Ø1UF	DISC
( )	C8	Ø.Ø1UF	DISC
( )	C9	Ø.Ø1UF	DISC
( )	C1Ø	25 UF	ELECTROLYTIC
( )	C11	Ø.Ø1UF	DISC
( )	C12	Ø.Ø1UF	DISC
( )	C13	25 UF	ELECTROLYTIC
( )	C14	Ø.Ø1UF	DISC
( )	C15	75ØPF	DISC

TRANSISTORS:

CHECK THE ERRATA SHEETS FOR TRANSISTOR ORIENTATION INSTRUCTIONS. THE ORIENTATION SHOWN ON THE ASSEMBLY DRAWING MAY NOT BE CORRECT FOR THE TRANSISTORS INCLUDED IN THIS KIT.

( )	Q1	2N3565	NPN HIB
( )	Q2	2N5135	NPN
( )	Q3	2N5138	PNP HIB

SOLDER AND CLIP THE CAPACITOR AND TRANSISTOR LEADS.

* THESE COMPONENTS ARE PART OF THE REMOTE CONTROL KIT.

INTEGRATED CIRCUITS:

WARNING: THE USE OF SOCKETS FOR MOUNTING THE INTEGRATED CIRCUITS IS NOT RECOMMENDED. MORE SPECIFICALLY, THE USE OF ANY IC SOCKETS NOT SUPPLIED BY PERCOM DATA CO. MAY VOID THE WARRANTY. IF YOU WISH TO USE SOCKETS, A KIT IS AVAILABLE FROM PERCOM. THESE SOCKETS ARE OF SUBSTANTIALLY HIGHER QUALITY THAN IS AVAILABLE THROUGH SURPLUS OUTLETS.

IF YOU ARE NOT FAMILIAR WITH INTEGRATED CURCUIT INSERTION AND SOLDERING TECHNIQUES, REFER TO APPENDIX A FOR HANDLING INSTRUCTIONS.

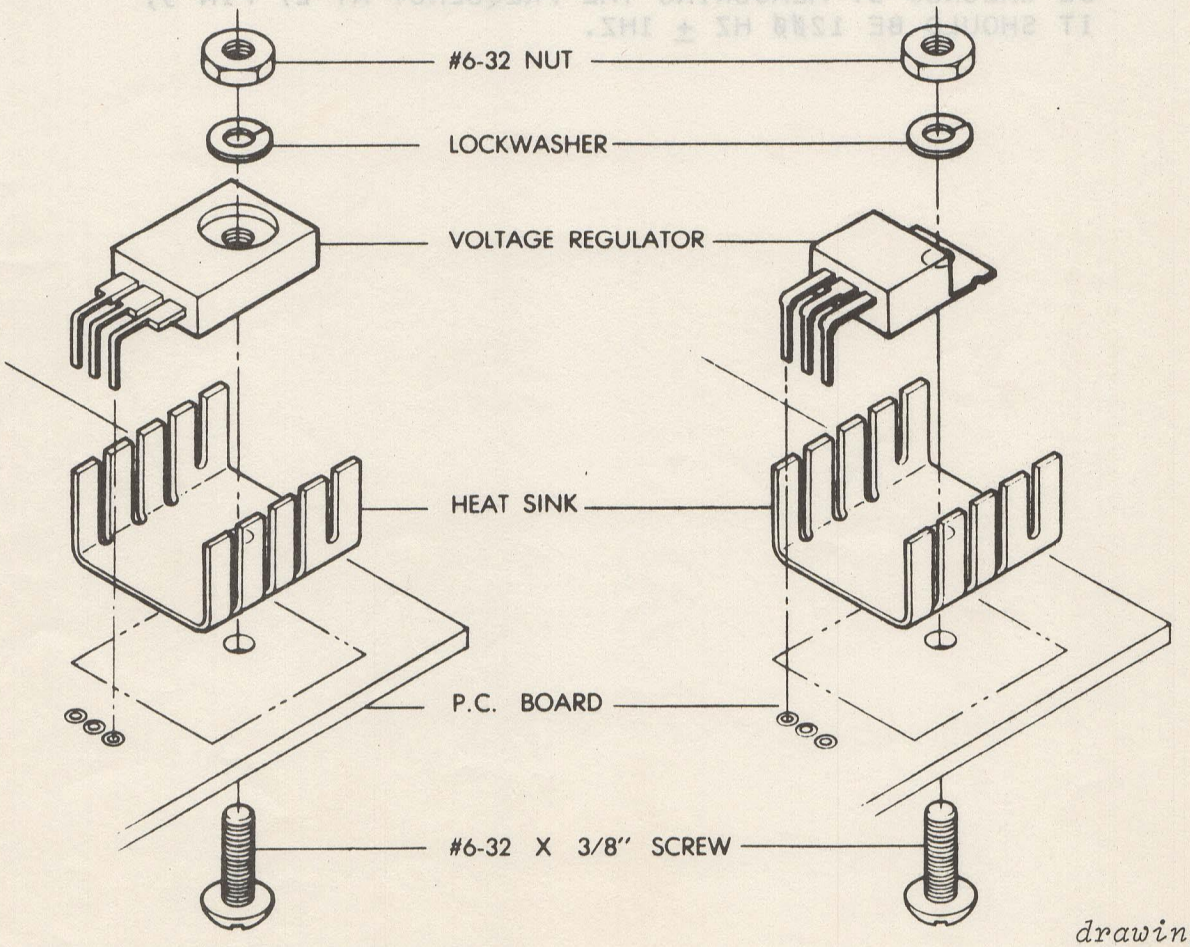
CHECK	IC	TYPE
( )	Z1	LM339
( )	Z2	74LS113
( )	Z3	74LS197
( )	Z4	74LS153
( )	Z5	74LS197
( )	Z6	74LS197
( )	Z7	74LS86
( )	Z8	74LS74
( )	Z9	74LS74
( )	Z1Ø	74LS157
( )	Z11	7474
( )	Z12	74LS1Ø
( )	Z13	74LS74
( )	Z14	74LSØ4
( )	Z15	74LSØØ
( )	Z16	74LSØØ
( )	Z17	25Ø2 OR AY5-1Ø13
( )	Z18	74LS197
( )	Z19	NOT USED (11Ø BAUD OPTION)
( )	Z2Ø	74LS3Ø
( )	Z21	74LSØ4
( )	Z22	74LSØ2
( )	Z23	74367
( )	Z24	74367
( )	Z25	74367

RECHECK ORIENTATION (NOTE THAT ALTERNATE ROWS OF IC'S ARE ORIENTED DIFFERENTLY) AND SOLDER ALL INTEGRATED CIRCUITS

MISC:

( ) 78Ø5 5 VOLT REGULATOR
PLACE THE METAL TAB OF THE REGULATOR OVER THE HOLE IN THE HEAT SINK AREA ON THE LOWER LEFT OF THE CIRCUIT CARD. POSITION THE THREE LEADS OVER THE LEAD FEED THRU HOLES AND NOTE WHERE TO BEND EACH LEAD. BEND EACH LEAD WITH SMALL PLIERS AND CHECK TO SEE THAT WHEN THE LEADS GO THROUGH THE BOARD, THE MOUNTING HOLES LINE UP. INSERT THE 6-32 SCREW FROM THE BOTTOM OF THE BOARD, PLACE THE HEAT SINK OVER THE SCREW FROM THE TOP, INSERT THE REGULATOR LEADS INTO THE BOARD WHILE THE TAB SLIPS OVER THE MACHINE SCREW. USE THE LOCKWASHER AND NUT TO SECURE THE REGULATOR AND HEAT SINK TO THE BOARD. SOLDER THE LEADS AND TRIM.

( ) RT 47K OR 5ØK TRIMMER RESISTOR
SOLDER IN PLACE
( ) TSA 1Ø CONTACT TERMINAL STRIP
( ) TSB 1Ø CONTACT TERMINAL STRIP
SOLDER IN PLACE
( ) CHECK THE ERRATA SHEET AGAIN FOR NECESSARY CHANGES TO THE CIRCUIT



BENDING THE VOLTAGE REGULATOR LEADS

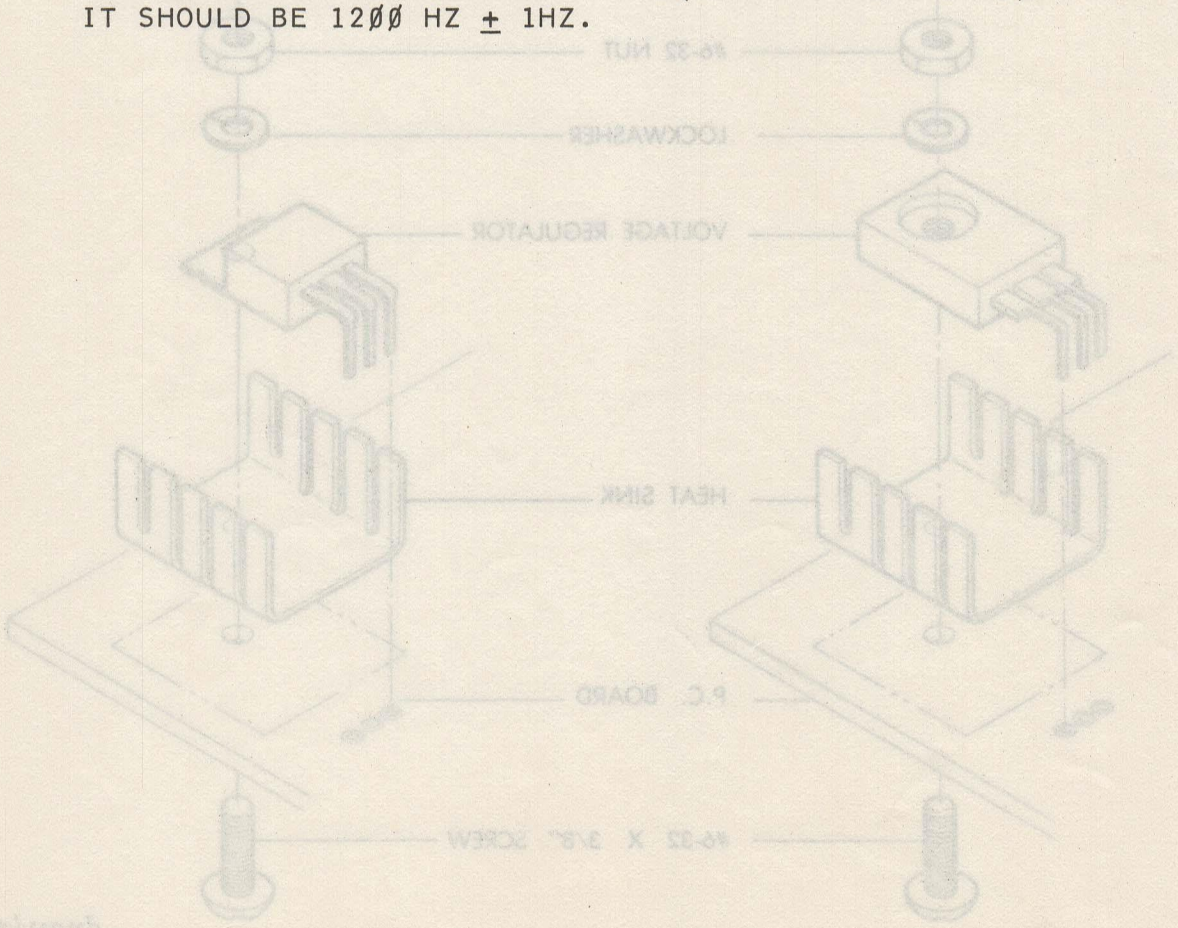
drawing by VectorGraphics

CIRCUIT ADJUSTMENT

IF THE CI-812 WAS ASSEMBLED FROM A KIT IT WILL BE NECESSARY TO ADJUST THE VCO TRIMMER (RT).

( ) INSTALL THE CI-812 INTO YOUR COMPUTER AND APPLY POWER (NO CONNECTION FROM THE CASSETTE PLAYER).
( ) MEASURE THE VOLTAGE AT TP1 (UPPER LEFT HAND CORNER OF CARD) WITH A HIGH IMPEDANCE (2ØK OHMS/VOLT) VOLTMETER (CONNECT THE VOLTMETER RETURN TO TSB-1Ø). IT SHOULD BE APPROXIMATELY 2 VOLTS, NOTE THE EXACT READING.
( ) WITH A CLIP LEAD OR PIECE OF WIRE JUMPER FROM THE BOTTOM END OF R17 TO THE TOP END OF C4.
( ) NOTE THE VOLTMETER READING WHILE ADJUSTING TRIMMER RT. AT SOME POINT IN THE ADJUSTMENT THE VCO WILL "JUMP INTO LOCK" AND THE VOLTAGE AT TP1 WILL FOLLOW THE POT ADJUSTMENT. ADJUST THE POT WHILE "IN LOCK" FOR THE SAME VOLTAGE AS WAS MEASURED EARLIER.
( ) REMOVE THE JUMPER.

IF A FREQUENCY COUNTER IS AVAILABLE THE ADJUSTMENT CAN BE CHECKED BY MEASURING THE FREQUENCY AT Z7 PIN 9; IT SHOULD BE 12ØØ HZ ± 1HZ.



CONNECTING TO THE CI-812:

CASSETTE RECORDER:

FORTUNATELY NEARLY ANY CASSETTE TAPE RECORDER WILL PERFORM WELL WITH CI-812. THE CASSETTE INTERFACE IS COMPATIBLE WITH THE EARPLUG OUTPUT AND AUX OR MIC INPUTS ON MOST PORTABLE CASSETTE RECORDERS. OTHER TYPES OF RECORDERS MAY REQUIRE SOME KIND OF AMPLIFIER BETWEEN THE RECORDER AND CI-812.

EARPLUG: CONNECT THE TAPE RECORDER EARPLUG TO TSA CONNECTOR PIN 5. CONNECT THE RETURN OR SHIELD TO TSA PIN 4 (GROUND).

AUX: CONNECT THE TAPE RECORDER AUX INPUT TO TSA CONNECTOR PIN 2. CONNECT THE RETURN OR SHIELD TO TSA PIN 3 (GROUND).

MIC: NORMALLY CONNECTION TO THE TAPE RECORDER MICROPHONE INPUT IS NOT NECESSARY. THE AUX INPUT IS PREFERRED SINCE IT OPERATES AT A HIGHER SIGNAL LEVEL AND IS LESS SENSITIVE TO NOISE PICKUP. IF THE MIC INPUT IS USED CONNECT TO THE TSA CONNECTOR PIN 1 (INSTEAD OF PIN 2). CONNECT THE RETURN SHIELD TO TSA PIN 3 (GROUND).

WARNING: SOME RECORDERS HAVE COMMON RETURN CIRCUITS ON THE EARPLUG AND INPUT JACKS WHICH MAY CAUSE GROUND LOOP HUM AND NOISE IF BOTH EARPLUG AND AUX (OR MIC) RETURNS ARE EXTERNALLY GROUNDED. IF THIS IS A PROBLEM, DISCONNECT THE AUX RETURN (SHIELD) AND LEAVE IT DISCONNECTED. THE EARPLUG RETURN WILL PROVIDE THE RETURN CIRCUIT. YOU WILL BE ABLE TO HEAR THE NOISE OR HUM IF A SPEAKER IS CONNECTED TO THE 'SIDETONE' OUTPUT (DESCRIBED LATER).

WARNING: SOME RECORDERS LEAVE THE BUILT-IN MICROPHONE ACTIVE EVEN IF A PLUG IS INSERTED INTO THE AUX JACK. THIS WILL ALLOW ROOM NOISE TO 'CLOBBER' YOUR RECORDING. USE THE MICROPHONE JACK OR STICK A 'DUMMY' PLUG INTO THE MICROPHONE JACK TO KILL THE BUILT-IN MICROPHONE.

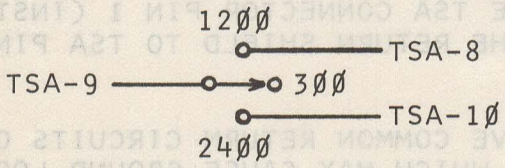
CASSETTE DATA RATE SELECTION:

THE PERCOM CI-812 CASSETTE INTERFACE IS CAPABLE OF OPERATING AT 3ØØ, 6ØØ, 12ØØ OR 24ØØ BAUD. THE DATA RATE IS SELECTED BY PINS 8 AND 1Ø ON THE TSA CONNECTOR. IF NO CONNECTION IS MADE TO EITHER PIN THE CASSETTE INTERFACE IS CONFIGURED FOR 3ØØ BAUD (K.C. STANDARD). FOR OTHER DATA RATES CONNECT THE PINS AS FOLLOWS:

TSA -8	TSA -1Ø	CASSETTE DATA RATE
NC*	NC	3ØØ BAUD
GND#	GND	6ØØ "
GND	NC	12ØØ "
NC	GND	24ØØ "

* NO CONNECTION
# GROUND IS AVAILABLE AT TSA-9

THE DATA RATE IS MOST EASILY CONTROLLED BY CONNECTING A SINGLE POLE 3-POSITION SWITCH AS FOLLOWS:



DATA TERMINAL:
THE CI-812 INCLUDES A FULL DUPLEX DATA TERMINAL INTERFACE AT RS-232 LEVELS FOR 3ØØ, 6ØØ, 12ØØ, 24ØØ, 48ØØ OR 96ØØ BAUD DATA TERMINALS.

( ) CONNECT THE KEYBOARD OR DATA TERMINAL TRANSMITTED DATA (EIA PIN 2) TO TSB-9.
( ) CONNECT THE PRINTER, DISPLAY OR DATA TERMINAL RECEIVED DATA (EIA PIN 3) TO TSB-8.
( ) CONNECT THE DATA TERMINAL SIGNAL RETURN (EIA PIN 7) TO TSB-1Ø. DO NOT CONNECT THE PROTECTIVE GROUND (EIA PIN 1) TO TSB-1Ø, IT SHOULD BE CONNECTED INSTEAD TO THE FRAME OF THE HOST COMPUTER.

THE DATA TERMINAL RATE IS DETERMINED BY AN APPROPRIATE JUMPER IN THE PADS BETWEEN Z9 AND Z1Ø. JUMPER ACROSS THE APPROPRIATE NUMBER. A 7 POLE DIP SWITCH MAY BE INSTALLED IN THE PADS IF DESIRED BUT ONLY ONE SWITCH MAY BE CLOSED AT ANYTIME.

ADDRESS SELECTION:

THE CI-812 RESPONDS TO I/O COMMANDS FROM THE PROCESSOR.

INPORT XXXXXXXØ TRANSFERS INTERFACE STATUS TO THE PROCESSOR.

OUTPORT XXXXXXXØ TRANSFERS CONTROL INSTRUCTIONS TO THE INTERFACE.

INPORT XXXXXXX1 TRANSFERS 8 BITS OF DATA FROM THE INTERFACE TO THE PROCESSOR.

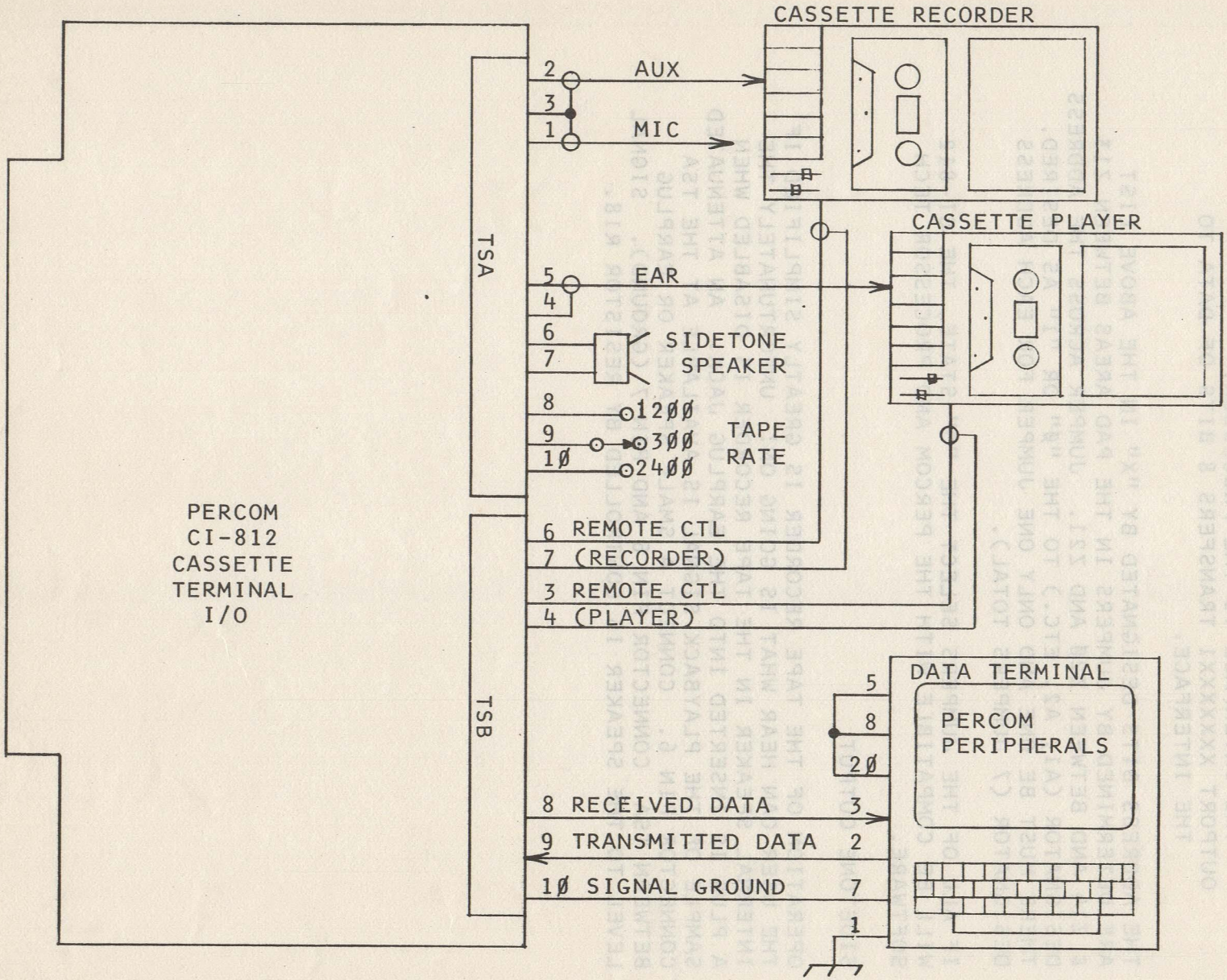
OUTPORT XXXXXXX1 TRANSFERS 8 BITS OF DATA TO THE INTERFACE.

THE ADDRESS BITS DESIGNATED BY "X" IN THE ABOVE LIST ARE DETERMINED BY JUMPERS IN THE PAD AREAS BETWEEN Z13 & Z14 AND BETWEEN Z2Ø AND Z21. JUMPER ACROSS THE ADDRESS DESIGNATOR (A1, A2, ETC.) TO THE "Ø" OR "1" AS DESIRED. THERE MUST BE ONE AND ONLY ONE JUMPER FOR EACH ADDRESS DESIGNATOR (7 JUMPERS TOTAL).

IF ALL OF THE JUMPERS SELECT THE "0" STATE, THE CI-812 WILL BE COMPATIBLE WITH THE PERCOM AND PROCESSOR TECH SOFTWARE.

SIDETONE OUTPUT

OPERATION OF THE TAPE RECORDER IS GREATLY SIMPLIFIED IF THE USER CAN HEAR WHAT IS GOING ON! UNFORTUNATELY THE INTERNAL SPEAKER IN THE TAPE RECORDER IS DISABLED WHEN A PLUG IS INSERTED INTO THE EARPLUG JACK. AN ATTENUATED SAMPLE OF THE PLAYBACK SIGNAL IS AVAILABLE AT THE TSA CONNECTOR PIN 6. CONNECT A SMALL SPEAKER OR EARPLUG BETWEEN TSA CONNECTOR PIN 6 AND PIN 7 (GROUND). SIGNAL LEVEL TO THE SPEAKER IS CONTROLLED BY RESISTOR R18.



SYSTEM CONFIGURATION

OPERATING PROCEDURE:

CASSETTE SELECTION AND CARE:

THE CHOICE OF CASSETTE TAPE HAS MORE EFFECT ON PERFORMANCE THAN ALL OTHER FACTORS COMBINED. GET THE VERY BEST TAPE YOU CAN BUY. ANYTHING LESS THAN THE BEST WILL RESULT IN MUCH FRUSTRATION. AVOID USING THE C9Ø AND C12Ø CASSETTES. THE TAPE IS TOO THIN AND FRAGILE. C6Ø AND SHORTER ARE MUCH MORE RUGGED AND RELIABLE.

IF THE CASSETTE IS NOT IN USE IT SHOULD BE STORED IN ITS CONTAINER IN A DUST FREE LOCATION. KEEP THE CASSETTE RECORDER SPOTLESSLY CLEAN. CLEAN THE HEAD, CAPSTAN, AND PINCH ROLLER WITH A CLEANING SOLUTION SUGGESTED BY THE EQUIPMENT MANUFACTURER. DO NOT SMOKE IN THE ROOM IN WHICH THE CASSETTE EQUIPMENT IS USED OR STORED.

IT IS IMPOSSIBLE TO ADEQUATELY STRESS THE IMPORTANCE OF BUYING THE VERY BEST QUALITY TAPE AND THEN KEEPING IT AND THE TAPE UNIT CLEAN.

IT IS RECOMMENDED EACH CASSETTE BE THOROUGHLY TESTED BEFORE USE. REFER TO APPENDIX C FOR INSTRUCTIONS.

RECORDING DATA ON TAPE:

1. DO NOT RECORD ON THE FIRST TWO FEET OF TAPE (15 SEC.). THE LEADER-TAPE SPLICE CAUSES A 'RIPPLE' ON ADJACENT LAYERS WHICH MAY CAUSE ERRORS.

2. PREPARE THE COMPUTER TO OUTPUT THE REQUIRED DATA TO THE CASSETTE INTERFACE. DO NOT BEGIN OUTPUTTING THE DATA JUST YET.

3. PLACE THE CASSETTE RECORDER IN RECORD MODE AND START THE TAPE. TURN ON THE AUTOMATIC LEVEL CONTROL OR ADJUST THE RECORDER FOR PROPER SIGNAL LEVEL.

4. ALLOW THE TAPE TO RUN FOR 3 TO 5 SECONDS. THE RECORDER WILL BE RECORDING A 24ØØ HZ 'LEADIN' TONE ON THE TAPE DURING THIS INTERVAL.

5. WHILE ALLOWING THE TAPE TO RUN, CAUSE THE COMPUTER TO BEGIN TRANSFERRING DATA TO THE CASSETTE INTERFACE.

6. WHEN THE RECORDING IS COMPLETE, LET THE TAPE RUN FOR A FEW SECONDS TO RECORD A 'LEADOUT' TONE.

PLAYBACK:

1. ADJUST THE PLAYBACK SIGNAL LEVEL FOR 4 TO 1Ø VOLTS PEAK-TO-PEAK. MARK THE VOLUME CONTROL SETTING FOR FUTURE REFERENCE. ADJUST THE TONE CONTROL (IF ONE EXISTS) FOR MAXIMUM RESPONSE. THE VOLUME SHOULD BE ADJUSTED WHILE PLAYING THE 24ØØ HZ 'LEADIN' TONE PRECEDING A BLOCK OF DATA.

2. LOCATE THE 'LEADIN' 24ØØ HZ TONE PRECEDING THE DESIRED BLOCK OF DATA. IF A SMALL SPEAKER IS CONNECTED TO THE 'SIDETONE' OUTPUT (TSA CONNECTOR PIN 6), THE TONE CAN BE HEARD WITHOUT PULLING OUT THE EARPLUG LEAD FROM THE CASSETTE PLAYER.

3. BEFORE THE CASSETTE BEGINS OUTPUTTING DATA, PREPARE THE COMPUTER TO ACCEPT THE DATA WHEN IT ARRIVES.

BE CERTAIN THE PLAYBACK IS ONE OR TWO SECONDS INTO THE 'LEADIN' TONE BEFORE ALLOWING THE COMPUTER TO ACCEPT THE PLAYBACK DATA. THIS IS TO AVOID READING THE 'RESIDUALS' FROM PREVIOUS RECORDINGS AND THE 'TRASH' CAUSED BY TURNING THE CASSETTE RECORDER ON AND OFF. SUFFICIENT TIME IS AVAILABLE TO PERFORM THE NECESSARY STEPS IF THE TAPE WAS RECORDED WITH A 3 TO 5 SECOND 'LEADIN' TONE.

4. IF THE RECORDED DATA HAS AN 'END-OF-BLOCK' CODE AT THE END OF THE RECORDED BLOCK OF DATA, THE COMPUTER CAN BE MADE TO AUTOMATICALLY IGNORE THE CASSETTE OUTPUT AFTER THE 'EOB' CODE. IF NO SUCH INDICATION EXISTS, THE USER WILL HAVE TO DISABLE THE COMPUTER BEFORE TURNING OFF THE TAPE TO PREVENT THE TURN-OFF TRANSIENT FROM SENDING CONFUSING 'TRASH' TO THE COMPUTER. OBVIOUSLY A DATA BLOCK TERMINATED WITH SOME FORM OF 'END-OF-BLOCK' INDICATION IS PREFERRED. THE PROGRAM LOADING SOFTWARE CONTAINED IN APPENDIX A PROVIDES PROPER BEGINNING OF BLOCK AND END OF BLOCK INDICATION.

REFER TO APPENDIX B FOR INFORMATION ON SEMIAUTOMATIC OPERATION USING THE CASSETTE RECORDER REMOTE CONTROL JACK.

SOFTWARE CONSIDERATIONS:

ATTACHED TO THIS SECTION ARE SEVERAL PROGRAMS WHICH ILLUSTRATE HOW TO USE THE CI-812. THESE PROGRAMS MAY BE USED IN WHOLE OR AS PART OF YOUR SPECIFIC CASSETTE OPERATING SYSTEM. THE DESIGN OF THE CI-812 IS SUCH THAT IT IS COMPATIBLE, INSOFAR AS POSSIBLE, WITH THE SOFTWARE AVAILABLE FROM PROCESSOR TECHNOLOGY AND IMS ASSOCIATES.

THE CI-812 CONTAINS A UART (UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER) WHICH IS USED TO SEND DATA TO AND RECEIVE DATA FROM THE CASSETTE TAPE UNIT(S) AND THE DATA TERMINAL.

THE UART STATUS IS AVAILABLE VIA INPUT PORT XXXXXXXØ THE "X" REPRESENTS ADDRESS SELECTION JUMPERS WHICH MUST BE INSTALLED ON THE CI-812 TO DETERMINE THE DESIRED ADDRESS TO WHICH THE CI-812 WILL RESPOND. THE PERCOM SOFTWARE IS WRITTEN ASSUMING ALL OF THE ADDRESS SELECTION JUMPERS ARE SET FOR "Ø".

INPUT PORT XXXXXXXØ BIT 7 IS UART TRANSMITTER BUFFER READY
" 6 IS UART RECEIVER DATA AVAILABLE
" 5 IS UART RECEIVER OVER RUN
" 4 IS UART RECEIVER FRAMING ERROR
" 3 IS UART RECEIVER PARITY ERROR
" 2 IS NOT USED
" 1 IS NOT USED
" Ø IS NOT USED

NORMALLY ONLY BIT 7 (TBMT) AND BIT 6 (DAV) WILL BE EXAMINED TO DETERMINE UART STATUS.

OUTPUT PORT XXXXXXXØ DETERMINES WHETHER THE UART WILL BE CLOCKED BY THE INTERNAL CLOCK AT THE SELECTED DATA TERMINAL OR CASSETTE DATA RATE OR BY THE CLOCK OBTAINED FROM THE CASSETTE TAPE DURING PLAYBACK. IT ALSO DETERMINES WHETHER THE UART RECEIVER WILL GET DATA FROM THE DATA TERMINAL OR FROM THE CASSETTE.

IF BIT Ø IS "ZERO":

A) THE UART RECEIVER WILL BE CONNECTED TO THE DATA TERMINAL (KEYBOARD)
B) THE CASSETTE PLAYBACK WILL BE IGNORED
C) RELAY K1 (IF INSTALLED) WILL BE OFF (DE-ENERGIZED)
D) THE UART RECEIVER AND TRANSMITTER WILL BE CLOCKED AT A RATE DETERMINED BY THE TERMINAL RATE STRAP ON THE CI-812

SOFTWARE CONT'D.

IF BIT Ø IS "ONE":

A) THE UART RECEIVER WILL BE CONNECTED TO THE CASSETTE DEMODULATOR FOR DATA INPUT

B) THE DATA TERMINAL KEYBOARD WILL BE IGNORED

C) RELAY K1 (IF INSTALLED) WILL BE ON

* D) THE UART RECEIVER WILL BE CLOCKED BY A SIGNAL DERIVED FROM THE TAPE RECORDED DATA (SELF CLOCKING)

E) THE UART TRANSMITTER WILL BE CLOCKED AT A RATE DETERMINED BY THE LEVELS ON THE CASSETTE RATE SELECTION INPUTS AT TSA-8 AND TSA-1Ø

* Cassette Rate selection inputs need to be considered.

IF BIT 1 IS A "ZERO":

A) RELAY K2 (IF INSTALLED) WILL BE OFF

B) THE UART TRANSMITTER WILL GENERATE ONLY ONE STOP BIT (TERMINAL MODE)

IF BIT 1 IS A "ONE":

A) RELAY K2 (IF INSTALLED) WILL BE ON

B) THE UART TRANSMITTER WILL GENERATE TWO STOP BITS (CASSETTE MODE)

BITS 2 THRU 7 ARE NOT USED.

THE LATCHES WHICH STORE BITS Ø AND 1 ARE SET TO "ZERO" BY A POWER-ON-CLEAR OR RESET FROM THE IMSAI COMPUTER FRONT PANEL.

BIT Ø IS USED PRIMARILY TO SWITCH THE UART BETWEEN THE DATA TERMINAL AND THE PLAYBACK CASSETTE.

BIT 1 IS USED TO CONTROL THE RECORDING CASSETTE (IN A TWO CASSETTE SYSTEM) AND DETERMINE THE NUMBER OF STOP BITS TRANSMITTED BY THE UART.

THE UART TRANSMITTER SENDS DATA TO THE DATA TERMINAL AND CASSETTE SIMULTANEOUSLY. HOWEVER, THE RATE IS CONTROLLED BY BIT Ø.

THE ABOVE SYSTEM GIVES CONSIDERABLE FLEXIBILITY FOR BOTH SINGLE AND DUAL CASSETTE SYSTEMS. STUDY IT CAREFULLY AND YOU WILL BE ABLE TO CONFIGURE A SYSTEM WHICH IS OPTIMUM FOR YOUR REQUIREMENTS.

SOFTWARE CONT'D.

TO SELECT THE DATA TERMINAL FOR DATA INPUT:

```
        XRA   A
        OUT   Ø
```

TO SELECT AND TURN ON THE CASSETTE FOR DATA INPUT:

```
        MVI   A,1
        OUT   Ø
```

TO TURN ON THE CASSETTE RECORDER (TERMINAL RATE)

```
        MVI   A,2
        OUT   Ø
```

PORT XXXXXXX1 TRANSFERS DATA TO/FROM THE UART

THE FOLLOWING ROUTINE ILLUSTRATES HOW TO READ A BYTE FROM THE CI-812.

```
LOOP    IN    Ø      TEST RECEIVER STATUS (DAV)
        ANI   4OH
        JZ    LOOP   DO AGAIN IF NOT READY
        IN    1      GET THE BYTE OR CHARACTER
        RET
```

TO RECORD OR OUTPUT A BYTE FROM THE PROCESSOR ACCUMULATOR:

```
        PUSH  PSW    SAVE THE BYTE
LOOP    IN    Ø      TEST TRANSMITTER STATUS (TBMT)
        ANI   8OH
        JZ    LOOP   DO AGAIN IF NOT READY
        POP   PSW    RESTORE THE BYTE
        OUT   1      OUTPUT THE BYTE
        RET
```

BOOTSTRAP LOADER

THE FOLLOWING PROGRAM IS SHORT ENOUGH TO BE CONVENIENTLY LOADED BY HAND USING THE FRONT PANEL SWITCHES ON YOUR ALTAIR OR IMSAI COMPUTER. IT LOADS ONE PAGE (256 BYTES) OF DATA AND IS DESIGNED TO OPERATE WITH THE PERCOM CI-812 CASSETTE I/O AND THE PERCOM TEST CASSETTE WHICH CONTAINS AN INTEL FORMAT CHECKSUM LOADER.

TO USE THIS PROGRAM WITH THE PERCOM TEST CASSETTE, LOAD THE PROGRAM BUT DO NOT START IT RUNNING. START THE CASSETTE TAPE AND LET IT RUN UNTIL YOU ARE ONE OR TWO SECONDS INTO THE NULL CODE LEADER. WHILE THE TAPE IS RUNNING START THE BOOTSTRAP PROGRAM (EXAMINE ADDRESS ØØØØ AND PRESS RUN). WHEN THE LOAD IS COMPLETED THE COMPUTER WILL AUTOMATICALLY BEGIN EXECUTING THE PROGRAM JUST LOADED.

Many IMSAI and ALTAIR Computers destroy the first memory location when reset. If this problem has not been corrected in your computer it will be necessary to relocate the Bootstrap Loader.

```
                    * PERCOM CASSETTE BOOTSTRAP LOADER (8Ø8Ø)*
ØØØØ  AF              XRA   A
ØØØ1  6F              MOV   L,A        INITIALIZE H&L
ØØØ2  67              MOV   H,A
ØØØ3  3C              INR   A
ØØØ4  D3 ØØ           OUT   Ø          SELECT  CASSETTE INPUT
ØØØ6  DB Ø1           IN    1          CLEAR UART
ØØØ8  31 1D ØØ        LXI   SP,STAK    SETUP RETURN ADDRESS
ØØØB  DB ØØ           IN    Ø          TEST UART STATUS (DAV)
ØØØD  E6 4Ø           ANI   4ØH
ØØØF  C8              RZ               RETURN-NOT READY
ØØ1Ø  DB Ø1           IN    1          GET DATA
ØØ12  24              INR   H          TEST H REGISTER
ØØ13  25              DCR   H
ØØ14  C2 19 ØØ        JNZ   STR        FIRST NON ZERO BYTE IS
ØØ17  67              MOV   H,A        PAGE ADDRESS
ØØ18  C9              RET
ØØ19  77        STR   MOV   M,A        STORE DATA BYTE
ØØ1A  2C              INR   L          BUMP LOAD ADDRESS
ØØ1B  CØ              RNZ              GET NEXT BYTE
ØØ1C  E9              PCHL             ALL DONE - NOW EXECUTE
ØØ1D  Ø8 ØØ           DW    RTN
```

BOOTSTRAP DUMP

THE FOLLOWING PROGRAM WILL RECORD A PAGE (256 BYTES) OF DATA ON CASSETTE IN A FORMAT WHICH MAY SUBSEQUENTLY BE LOADED INTO THE COMPUTER USING THE BOOTSTRAP LOADER DESCRIBED ON THE PREVIOUS PAGE. SET THE DESIRED PAGE ADDRESS UP ON THE FRONT PANEL SWITCHES (SWITCHES 15 THRU 8 ON THE IMS COMPUTER), START THE PROGRAM RUNNING, START THE CASSETTE RECORDING. LET THE TAPE RUN FOR ABOUT 1Ø-15 SECONDS TO RECORD A NULL CODE LEADER THEN PRESS ANY KEY ON YOUR TERMINAL KEYBOARD. AT 3ØØ BAUD IT TAKES APPROXIMATELY 9 SECONDS TO RECORD A 256 BYTE PAGE. LET THE TAPE RUN AN ADDITIONAL 2-3 SECONDS TO ASSURE A CLEAN RUN OUT.

THE DATA TERMINAL RATE SELECTION STRAP MUST BE SET AT THE RATE YOU WISH THE DATA TO BE RECORDED ON CASSETTE.

```
                * PERCOM CASSETTE BOOTSTRAP DUMP (8Ø8Ø) *

3D7D  31 FF CF          LXI   SP,SPTR   INITIALIZE STACK POINTER
3D8Ø  DB Ø1             IN    1         CLEAR UART
3D82  AF          B1    XRA   A
3D83  6F              MOV   L,A         INITIALIZE L
3D84  D3 ØØ           OUT   Ø           SELECT TERMINAL
3D86  CD A5 3D        CALL  OUT         OUTPUT NULL CODE
3D89  DB ØØ           IN    Ø           TEST KEYBOARD STATUS
3D8B  E6 4Ø           ANI   4ØH
3D8D  CA 82 3D        JZ    B1          DO ANOTHER NULL
3D9Ø  DB Ø1           IN    1           CLEAR UART
3D92  DB FF           IN    FF          GET PAGE ADDRESS FROM
3D94  D3 FF           OUT   FF          PANEL SWITCHES - ECHO
3D96  67              MOV   H,A         STORE IN H REG
3D97  CD A5 3D        CALL  OUT         OUTPUT PAGE ADDRESS
3D9A  7E          B2  MOV   A,M         GET DATA
3D9B  CD A5 3D        CALL  OUT         OUTPUT
3D9E  2C              INR   L           BUMP ADDRESS
3D9F  C2 9A 3D        JNZ   B2          GET ANOTHER BYTE
3DA2  C3 82 3D        JMP   B1          BACK TO NULL

3DA5  5F          OUT MOV   E,A         SAVE BYTE
3DA6  DB ØØ       T1  IN    Ø           TEST STATUS (TBMT)
3DA8  E6 8Ø           ANI   8ØH
3DAA  CA A6 3D        JZ    T1          KEEP TESTING UNTIL READY
3DAD  7B              MOV   A,E         RESTORE BYTE
3DAE  D3 Ø1           OUT   1
3DBØ  C9              RET
```

PERCOM 8Ø8Ø MONITOR

THE FOLLOWING PROGRAM IS A CASSETTE OPERATING SYSTEM FOR A COMPUTING SYSTEM CONSISTING OF AN 8Ø8Ø (OR Z-8Ø) PROCESSOR, PERCOM CI-812 CASSETTE/TERMINAL I/O, AND A 3ØØ-96ØØ BAUD DATA TERMINAL.

THE PROGRAM IS AVAILABLE ON THE PERCOM TEST CASSETTE WHICH ALSO CONTAINS TEST PATTERNS TO VERIFY THE OPERATION OF THE CASSETTE INTERFACE. IT IS ALSO AVAILABLE ON PROM (17Ø2A OR 52Ø4).

THE PROGRAM STARTS WITH A "PHANTOM JUMP" WHICH WILL PERMIT IT TO BE USED ON COMPUTERS WHICH DO NOT HAVE FRONT PANEL SWITCHES. WE USE THIS PROGRAM WITH THE VECTORGRAPHICS PROM/RAM CARD WHICH HAS PROVISION FOR A PHANTOM JUMP START.

WHEN INITIALIZED, THE OPERATING SYSTEM PROMPTS THE USER WITH A QUESTION MARK (?).

EXAMINE MEMORY: (M)

TO EXAMINE A MEMORY LOCATION, TYPE M, THE ADDRESS LOCATION YOU WISH TO EXAMINE, AND A CARRIAGE RETURN. THE PRINTER WILL RESPOND WITH A RETYPE OF THE ADDRESS AND THE CONTENT OF THAT LOCATION.

YOU MAY EXAMINE SUCCESSIVE MEMORY LOCATIONS BY TYPING N.

TO EXAMINE A RANGE OF MEMORY, TYPE M, THE FIRST ADDRESS, SPACE, THE FINISH ADDRESS, AND A CARRIAGE RETURN.

CHANGE MEMORY: (C)

TO CHANGE A MEMORY LOCATION, FIRST EXAMINE THE LOCATION AS DESCRIBED EARLIER THEN TYPE C. THE PRINTER WILL RETYPE THE LOCATION ADDRESS AND WAIT FOR YOUR CHANGE. YOU MAY CHANGE SUCCESSIVE LOCATIONS BY TYPING A SPACE BETWEEN EACH ENTRY. WHEN YOU WISH TO QUIT, HIT CARRIAGE RETURN.

IF YOU MAKE AN ERROR AND DISCOVER IT BEFORE TYPING THE SPACE OR CARRIAGE RETURN, TYPE A SLASH (/). THE PRINTER WILL TYPE THE CURRENT ADDRESS AND GIVE YOU ANOTHER CHANCE. IF YOU HAVE TYPED THE SPACE, TYPE A CARRIAGE RETURN AND START AGAIN AT THE LOCATION IN ERROR.

LOAD A PROGRAM: (L)

TO LOAD A PROGRAM WHICH IS ON CASSETTE IN INTEL ASCII HEX FORMAT, TYPE L. DURING THE LOAD THE PROGRAM CHECKS TO MAKE SURE THE DATA IS BEING WRITTEN INTO MEMORY CORRECTLY. IF AN ERROR OCCURS THE PROGRAM ABORTS THE LOAD, STOPS THE TAPE (IF REMOTE CONTROL OPTION EXISTS) AND TYPES AN M FOLLOWED BY THE MEMORY ADDRESS WHICH DID NOT LOAD CORRECTLY. THIS WILL OCCUR IF YOU TRY TO LOAD INTO A ROM OR INTO A LOCATION WHERE THERE IS NO MEMORY OR IF THE MEMORY IS DEFECTIVE.

THE PROGRAM ALSO WATCHES FOR CHECKSUM ERRORS. IF A CHECKSUM ERROR OCCURS, THE PRINTER WILL TYPE AN X AND THE LAST ADDRESS LOADED.

YOU CAN USUALLY STOP THE TAPE, EJECT THE CASSETTE AND EXAMINE FOR CONTAMINATES. A PHOTOGRAPHERS AIR BULB IS USEFUL FOR BLOWING OFF DUST AND LINT. REINSTALL THE CASSETTE, REWIND A SHORT DISTANCE, AND START THE LOAD AGAIN. IF IT FAILS AT THE SAME POINT AGAIN, THE TAPE (OR RECORDING) IS DEFECTIVE.

VERIFY: (V)

VERIFY WORKS THE SAME AS A LOAD EXCEPT THAT DATA IS NOT WRITTEN INTO MEMORY IT IS COMPARED WITH THE EXISTING MEMORY CONTENT. IF A MISMATCH OCCURS, THE PRINTER PRINTS AN M AND THE ADDRESS OF THE MISMATCH.

DUMP A PROGRAM: (D)

TO DUMP A SECTION OF MEMORY ONTO TAPE IN THE RE-LOADABLE INTEL ASCII HEX FORMAT, TYPE D, THE START ADDRESS, A SPACE, THE FINISH ADDRESS, AND A CARRIAGE RETURN.

EXECUTE A PROGRAM: (G)

TO SEND THE PROGRAM COUNTER TO A DESIRED PROGRAM TO COMMENCE PROGRAM EXECUTION, TYPE G, THE EXECUTION ADDRESS, AND A CARRIAGE RETURN.

WHEN ENTERING DATA AND ADDRESS INFORMATION FROM THE KEYBOARD IT IS NOT NECESSARY TO TYPE LEADING ZEROS.

NOTICE: IN THIS PROGRAM, THE RATE AT WHICH DATA IS RECORDED ON CASSETTE IS THE SAME AS THE SELECTED DATA TERMINAL RATE. THE PROGRAM <u>DOES NOT</u> SWITCH TO THE CASSETTE RATE WHEN DUMPING TO CASSETTE.

```
                    * PERCOM 8Ø8Ø MONITOR*

CØØØ  C3 Ø3 CØ            JMP   STRT        PHANTOM JUMP
CØØ3  DB Ø1       STRT     IN    1           CLEAR UART RECEIVER
CØØ5  31 FF CF            LXI   SP,SPTR     SET STACK POINTER
CØØ8  CD ØE CØ            CALL  MON
CØØB  C3 Ø3 CØ            JMP   STRT
CØØE  AF          MON     XRA   A           SELECT TERMINAL KEYBOARD
CØØF  D3 ØØ               OUT   Ø
CØ11  CD DE C1            CALL  CRLF
CØ14  3E 3F               MVI   A, '?'
CØ16  CD CE C1            CALL  TTYO
CØ19  CD 9F C1            CALL  CIN         GET COMMAND CHARACTER
CØ1C  F5                  PUSH  PSW
CØ1D  CD CC C1            CALL  SPCE
CØ2Ø  F1                  POP   PSW
CØ21  FE 44               CPI   'D'
CØ23  CA 92 CØ            JZ    DUMP        RELOADABLE PROGRAM DUMP
CØ26  FE 4E               CPI   'N'
CØ28  CA 8E CØ            JZ    NXT         EXAMINE NEXT LOCATION
CØ2B  FE 4C               CPI   'L'
CØ2D  CA Ø3 C1            JZ    LOAD        LOAD PROGRAM
CØ3Ø  FE 56               CPI   'V'
CØ32  CA Ø3 C1            JZ    LOAD        VERIFY LOAD
CØ35  FE 4D               CPI   'M'
CØ37  CA 46 CØ            JZ    MEM         EXAMINE MEMORY
CØ3A  FE 43               CPI   'C'
CØ3C  CA 67 CØ            JZ    CNG         CHANGE MEMORY
CØ3F  FE 47               CPI   'G'
CØ41  CØ                  RNZ
CØ42  CD C8 CØ            CALL  AHEX        GET EXECUTION ADDRESS
CØ45  E9                  PCHL
                    * MEMORY DISPLAY*
CØ46  CD DD CØ     MEM    CALL  SETUP       GET START/FINISH ADDRESS
CØ49  CD EF CØ     M1     CALL  LNTH        CALCULATE LENGTH
CØ4C  AF                  XRA   A           CHECK FOR ZERO LENGTH
CØ4D  B8                  CMP   B
CØ4E  C8                  RZ                QUIT IF ZERO
CØ4F  CD 5Ø C1            CALL  ADD         OUTPUT ADDRESS
CØ52  CD CC C1            CALL  SPCE        SPACE
CØ55  CD CC C1     M2     CALL  SPCE        SPACE
CØ58  7E                  MOV   A,M         GET DATA
CØ59  CD AD C1            CALL  HEXOUT      CONVERT TO ASCII HEX-OUTPUT
CØ5C  23                  INX   H           BUMP MEMORY ADDRESS
CØ5D  Ø5                  DCR   B           DECREMENT BYTE COUNT
CØ5E  C2 55 CØ            JNZ   M2          NOT DONE? - DO AGAIN
CØ61  CD DE C1            CALL  CRLF        CARRIAGE RETURN, LINE FEED
CØ64  C3 49 CØ            JMP   M1          DO NEXT LINE
                    * CHANGE MEMORY*
CØ67  2B           CNG    DCX   H           POSITION MEMORY ADDRESS
CØ68  Ø6 1Ø        C1     MVI   B,1ØH       SET UP BYTE COUNT
CØ6A  CD DE C1            CALL  CRLF
CØ6D  CD 5Ø C1            CALL  ADD         OUTPUT CURRENT ADDRESS
CØ7Ø  CD CC C1            CALL  SPCE        DOUBLE SPACE
```

```
C073  CD CC C1          CALL  SPCE
C076  EB          C2    XCHG
C077  CD C8 C0          CALL  AHEX        GET NEW DATA
C07A  EB                XCHG
C07B  FE 2F             CPI   '/'        SLASH MEANS "ABORT THIS
C07D  CA 68 C0          JZ    C1         CHANGE AND DO AGAIN"
C080  73                MOV   M,E        STORE DATA IN MEMORY
C081  23                INX   H          BUMP MEMORY ADDRESS
C082  54                MOV   D,H        SAVE MEMORY ADDRESS
C083  5D                MOV   E,L
C084  FE 0D             CPI   0DH        CHECK FOR CARRIAGE RETURN
C086  C8                RZ               QUIT IF CR
C087  05                DCR   B          DECREMENT BYTE COUNT
C088  C2 76 C0          JNZ   C2         NOT ZERO? - GET ANOTHER BYTE
C08B  C3 68 C0          JMP   C1         START A NEW LINE

C08E  13          NXT   INX   D          UPDATE LIMIT ADDRESS
C08F  C3 49 C0          JMP   M1         EXAMINE NEXT MEMORY LOCATION
                  * CHECKSUM DUMP PROGRAM*
C092  CD DD C0    DUMP  CALL  SETUP      GET START/FINISH ADDRESS
C095  3E 02             MVI   A,02H      TURN ON CASSETTE RECORDER
C097  D3 00             OUT   0
C099  CD DE C1    D1    CALL  CRLF
C09C  0E 00             MVI   C,0        CLEAR CHECKSUM
C09E  3E 3A             MVI   A,':'      GET BLOCK HEADER
C0A0  CD CE C1          CALL  TTYO       OUTPUT
C0A3  CD EF C0          CALL  LNTH       CALCULATE BLOCK LENGTH
C0A6  78                MOV   A,B
C0A7  CD AD C1          CALL  HEXOUT     OUTPUT
C0AA  CA DE C1          JZ    CRLF       QUIT IF ZERO LENGTH
C0AD  CD 50 C1          CALL  ADD        OUTPUT ADDRESS
C0B0  AF                XRA   A
C0B1  CD AD C1          CALL  HEXOUT     OUTPUT BLOCK TYPE (00)
C0B4  7E          D2    MOV   A,M        GET DATA
C0B5  CD AD C1          CALL  HEXOUT     OUTPUT
C0B8  23                INX   H          BUMP MEMORY ADDRESS
C0B9  05                DCR   B          DECREMENT BYTE COUNT
C0BA  C2 B4 C0          JNZ   D2         NOT ZERO?-GET ANOTHER BYTE
C0BD  AF                XRA   A
C0BE  91                SUB   C          CALCULATE CHECKSUM
C0BF  CD AD C1          CALL  HEXOUT     OUTPUT CHECKSUM
C0C2  C3 99 C0          JMP   D1         START A NEW LINE
                  * INPUT ASCII - CONVERT TO BINARY*
C0C8  21 00 00    AHEX  LXI   H,0        CLEAR H AND L
C0CB  CD 9F C1    A1    CALL  CIN        INPUT A CHARACTER
C0CE  FE 30             CPI   '0'        RETURN IF CHARACTER IS
C0D0  D8                RC               ASCII '0' OR LESS
C0D1  29                DAD              SHIFT H AND L LEFT
C0D2  29                DAD              4 PLACES
C0D3  29                DAD
C0D4  29                DAD
C0D5  CD 97 C1          CALL  HEX        CONVERT CHAR TO BINARY
C0D8  85                ADD   L          COMBINE WITH PREVIOUS
C0D9  6F                MOV   L,A        RESULT
```

```
C0DA  C3 CB C0          JMP   A1          DO AGAIN

C0DD  CD C8 C0  SETUP   CALL  AHEX        GET START ADDRESS
C0E0  5D                MOV   E,L         SAVE IN D AND E
C0E1  54                MOV   D,H
C0E2  FE 0D             CPI   0DH         CHECK FOR CR
C0E4  CA EB C0          JZ    S1          RETURN IF CR VIA CRLF
C0E7  CD C8 C0          CALL  AHEX        GET FINISH ADDRESS
C0EA  EB                XCHG
C0EB  13        S1      INX   D           ADJUST FINISH ADDRESS
C0EC  C3 DE C1          JMP   CRLF        RETURN VIA CRLF
                * CALCULATE BLOCK LENGTH *
C0EF  7B        LNTH    MOV   A,E
C0F0  95                SUB   L
C0F1  47                MOV   B,A
C0F2  7A                MOV   A,D
C0F3  9C                SBB   H
C0F4  3E 10             MVI   A,10H
C0F6  C2 FB C0          JNZ   L1
C0F9  B8                CMP   B
C0FA  D0                RNC
C0FB  47        L1      MOV   B,A
C0FC  C9                RET
                ***CASSETTE CHECKSUM LOADER***
C100  31 FF CF          LXI   SP, SPTR
C103  57        LOAD    MOV   D, A
C104  3E 01             MVI   A, 01H
C106  D3 00             OUT   0
C108  CD 9F C1  READ    CALL  CIN         CHECK FOR BLOCK HEADER
C10B  FE 3A             CPI   ':'
C10D  C2 08 C1          JNZ   READ
C110  0E 00             MVI   C,0         CLEAR CHECKSUM
C112  CD 80 C1          CALL  CHAR        GET BLOCK LENGTH
C115  47                MOV   B,A
C116  CA 58 C1          JZ    HXND        QUIT IF ZERO LENGTH
C119  CD 80 C1          CALL  CHAR        GET ADDRESS (MSB)
C11C  67                MOV   H, A
C11D  CD 80 C1          CALL  CHAR        GET ADDRESS (LSB)
C120  6F                MOV   L,A
C121  CD 80 C1          CALL  CHAR        THROW AWAY BLOCK TYPE
C124  CD 80 C1  LOOP    CALL  CHAR        GET DATA
C127  5F                MOV   E, A
C128  7A                MOV   A, D        IS THIS A VERIFY?
C129  FE 56             CPI   'V'
C12B  7B                MOV   A, E
C12C  CA 30 C1          JZ    L1          VERIFY BYPASS
C12F  77                MOV   M, A        WRITE DATA TO MEMORY
C130  BE        L1      CMP   M           CHECK THE WRITE
C131  1E 4D             MVI   E,'M'       ERROR MESSAGE
C133  C2 43 C1          JNZ   ERR
C136  23                INX   H           BUMP MEMORY POINTER
C137  05                DCR   B           BUMP BLOCK LENGTH
C138  C2 24 C1          JNZ   LOOP        NOT DONE?  DO AGAIN
```

```
C13B  CD 8Ø C1          CALL  CHAR        GET CHECKSUM
C13E  1E 58             MVI   E, 'X'      ERROR MESSAGE
C14Ø  CA Ø8 C1          JZ    READ        NO ERROR? DO NEXT BLOCK
                  ***ERROR PRINTOUT***
C143  AF          ERR   XRA   A           TURN OFF CASSETTE
C144  D3 ØØ            OUT   Ø
C146  CD DE C1          CALL  CRLF
C149  7B                MOV   A, E        PRINT ERROR MESSAGE
C14A  CD CE C1          CALL  TTYO
C14D  CD CC C1          CALL  SPCE        RETURN VIA SPACE
C15Ø  7C          ADD   MOV   A, H        OUTPUT ADDRESS
C151  CD AD C1          CALL  HEXOUT
C154  7D                MOV   A, L
C155  C3 AD C1          JMP   HEXOUT
C158  7A          HXND  MOV   A, D        CHECK FOR READ MODE
C159  FE 52             CPI   'R'         (NO EXECUTION)
C15B  C8                RZ
C15C  CD 9F C1          CALL  CIN         RETURN IF CR
C15F  FE ØD             CPI   ØDH
C161  C8                RZ
C162  CD 83 C1          CALL  CHAR1       GET EXECUTION ADDRESS
C165  67                MOV   H, A
C166  CD 8Ø C1          CALL  CHAR
C169  6F                MOV   L, A
C16A  CD 8Ø C1          CALL  CHAR        CHECK CHECKSUM
C16D  1E 58             MVI   E, 'X'
C16F  C2 43 C1          JNZ   ERR         CHECKSUM ERROR
C172  AF                XRA   A           TURN OFF CASSETTE
C173  D3 ØØ             OUT   Ø
C175  F1                POP   PSW
C176  E9                PCHL              EXECUTE
                  ***GET 2 CHAR & CONVERT TO BINARY BYTE***
C18Ø  CD 9F C1    CHAR  CALL  CIN
C183  CD 97 C1    CHAR1 CALL  HEX
C186  Ø7                RLC
C187  17                RAL
C188  17                RAL
C189  17                RAL
C18A  5F                MOV   E, A
C18B  CD 9F C1          CALL  CIN
C18E  CD 97 C1          CALL  HEX
C191  83                ADD   E
C192  5F                MOV   E, A
C193  81                ADD   C
C194  4F                MOV   C, A
C195  7B                MOV   A, E
C196  C9                RET
C197  D6 3Ø       HEX   SUI   3ØH
C199  FE ØA             CPI   ØAH
C19B  D8                RC
C19C  D6 Ø7             SUI   Ø7H
C19E  C9                RET
C19F  DB ØØ       CIN   IN    Ø           TERMINAL/CASSETTE INPUT
```

```
C1A1  E6 4Ø          ANI   4ØH
C1A3  CA 9F C1       JZ    CIN
C1A6  DB Ø1          IN    1
C1A8  D3 Ø1          OUT   1
C1AA  E6 7F          ANI   7FH
C1AC  C9             RET
                  * CONVERT BYTE TO 2 ASCII HEX CHAR*
C1AD  F5          HEXOUT PUSH PSW
C1AE  ØF               RRC
C1AF  ØF               RRC
C1BØ  ØF               RRC
C1B1  ØF               RRC
C1B2  CD BE C1         CALL  HEXO
C1B5  F1               POP   PSW
C1B6  F5               PUSH  PSW
C1B7  CD BE C1         CALL  HEXO
C1BA  F1               POP   PSW
C1BB  81               ADD   C
C1BC  4F               MOV   C, A
C1BD  C9               RET
C1BE  E6 ØF       HEXO ANI   ØFH
C1CØ  C6 3Ø            ADI   3ØH
C1C2  FE 3A            CPI   3AH
C1C4  DA CE C1         JC    TTYO
C1C7  C6 Ø7            ADI   Ø7H
C1C9  C3 CE C1         JMP   TTYO
C1CC  3E 2Ø       SPCE MVI   A, 2ØH
C1CE  F5          TTYO PUSH  PSW          TERMINAL/CASSETTE OUTPUT
C1CF  DB ØØ       TI   IN    Ø
C1D1  Ø7               RLC
C1D2  D2 CF C1         JNC   T1
C1D5  Ø7 ØØ            RLC   NOP  <- WHY?
C1D7  DA Ø3 CØ         JC    STRT
C1DA  F1               POP   PSW
C1DB  D3 Ø1            OUT   1
C1DD  C9               RET
C1DE  3E ØD       CRLF MVI   A, ØDH
C1EØ  CD CE C1         CALL  TTYO
C1E3  3E ØA            MVI   A, ØAH
C1E5  CD CE C1         CALL  TTYO
C1E8  AF               XRA   A
C1E9  C3 CE C1         JMP   TTYO
```

THEORY OF OPERATION

REFER TO THE SCHEMATIC DIAGRAM THROUGHOUT THE FOLLOWING DESCRIPTION.

SHEET 1 OF THE SCHEMATIC IS THE CASSETTE AND TERMINAL INTERFACE CIRCUIT; SHEET 2 IS THE INTERFACE TO THE ALTAIR (S-1ØØ) BUS.

RECORD CIRCUIT:

THE UART (Z-17) IS THE PRIMARY INTERFACE BETWEEN THE COMPUTER BUS AND THE CASSETTE AND TERMINAL INTERFACE. THE TRANSMITTER SECTION OF THE UART RECEIVES PARALLEL DATA FROM THE PROCESSOR BUS VIA BUFFERS Z23 AND Z24 AND TRANSMITS SERIALLY TO THE DATA TERMINAL (VIA THE RS-232 INTERFACE CIRCUIT Z3 AND RELATED RESISTORS) AND TO THE CASSETTE MODULATOR Z2. Z15-A INVERTS THE SERIAL DATA FROM THE UART. WHEN Z15-3 IS LOW, J-K FLIP-FLOP Z2-A IS PREVENTED FROM TOGGLING AND THE Q OUTPUT IS FORCED TO THE HIGH STATE. Z2-B DIVIDES THE 48ØØHZ CLOCK BY TWO PRODUCING A 24ØØ HZ SQUARE WAVE AT Z2-9. WHEN Z15-3 IS HIGH, FLIP-FLOP Z2-A IS PERMITTED TO TOGGLE WHICH INHIBITS THE TOGGLING OF Z2-B ON EVERY OTHER CLOCK PULSE. THE NET RESULT IS THAT THE OUTPUT OF Z2-9 IS NOW A 12ØØ HZ SQUARE WAVE. WHEN DATA FROM THE UART IS A LOGIC ONE BIT, A 24ØØ HZ SIGNAL IS GENERATED AND WHEN THE DATA IS A LOGIC ZERO, A 12ØØ HZ SIGNAL IS GENERATED.

THE UART TRANSMITTER IS CLOCKED BY A SIGNAL DERIVED FROM THE PROCESSOR 2MHZ OSCILLATOR. THE RATE MAY BE CONTROLLED BY THE TERMINAL RATE STRAPPING OR BY THE CASSETTE RATE SELECTION AT TSA-8 AND TSA-1Ø. MULTIPLEXER Z1Ø-C DETERMINES WHICH SELECTION WILL CLOCK THE UART. IF FLIP-FLOP LATCH Z11-B IS SET, THE UART TRANSMITTER WILL BE CLOCKED BY THE OUTPUT OF MULTIPLEXER Z4-A WHICH IS CONTROLLED BY THE CASSETTE RATE SELECTION. IF Z11-B IS RESET, THE UART TRANSMITTER WILL BE CLOCKED AT THE RATE DETERMINED BY THE "TERMINAL RATE" STRAP. Z11-B IS SET OR RESET BY AN OUTPUT INSTRUCTION FROM THE PROCESSOR.

THE UART TRANSMITTER OUTPUTS A SERIAL BIT STREAM CONSISTING OF A START BIT, EIGHT DATA BITS, AND ONE OR MORE STOP BITS. THE MINIMUM NUMBER OF STOP BITS PRODUCED IS CONTROLLED BY Z11-A. WHEN Z11-A IS RESET THE UART TRANSMITTER WILL PRODUCE AS FEW AS ONE STOP BIT. THIS IS THE NORMAL MODE FOR OUTPUTTING DATA TO THE TERMINAL. TO MINIMIZE CASSETTE "OVERSPEED" PROBLEMS, DATA RECORDED ON CASSETTE SHOULD HAVE A MINIMUM OF TWO STOP BITS. IF Z11-A IS SET, THE UART TRANSMITTER WILL PRODUCE A MINIMUM OF TWO STOP BITS. Z11-A IS SET OR RESET BY AN OUTPUT INSTRUCTION FROM THE PROCESSOR.

THE TIMING OF THE UART IS SUCH THAT AT 3ØØ BAUD, A LOGIC ONE DATA BIT IS 8 CYCLES OF 24ØØ HZ AND A LOGIC ZERO BIT IS 4 CYCLES OF 12ØØ HZ. AT THE HIGHER DATA RATES, THE 24ØØ HZ AND 12ØØ HZ TONES REMAIN BUT THE NUMBER OF CYCLES PER DATA BIT IS PROGRESSIVELY REDUCED UNTIL AT 24ØØ BAUD A LOGIC ONE IS ONE CYCLE OF 24ØØ HZ AND A LOGIC ZERO IS ONE HALF CYCLE OF 12ØØ HZ. THIS IS THE POPULAR MANCHESTER OR BIPHASE CODE.

THE SQUARE WAVE IS FILTERED AND ATTENUATED BY R15, R16, R17, C5 AND IS FED TO THE AUXILIARY OR MICROPHONE INPUTS OF THE CASSETTE RECORDER.

THE MODULATOR CLOCK (48ØØ HZ) IS DERIVED FROM THE 2MHZ SOURCE ON THE PROCESSOR CARD.

PLAYBACK CIRCUIT:

THE SIGNAL FROM THE TAPE PLAYER EARPHONE OUTPUT IS SHAPED INTO A SQUARE WAVE BY SIGNAL CONDITIONER Z1-C, R7, R8 AND RELATED COMPONENTS. EXCLUSIVE - OR GATE Z7-A, R26, AND C6 CONVERT THE SQUARE WAVE INTO A STRING OF NARROW PULSES. Z6 AND Z13 RECOVER THE DATA, Z8 RECOVERS THE TIMING INFORMATION (CLOCK).

Z6 IS A "DEAD-ENDED" DIVIDER. IT BEHAVES AS A RETRIGGERABLE ONE-SHOT. WHEN THE 24ØØ HZ SIGNAL IS RECEIVED, THE DIVIDER IS CONSTANTLY RESET (RETRIGGERED) BEFORE IT IS ALLOWED TO "DEAD-END" (TIME OUT). THIS CAUSES Z13-5 (Q OUTPUT) TO REMAIN HIGH. WHEN THE 12ØØ HZ SIGNAL IS RECEIVED, THE DIVIDER IS ALLOWED TO DEAD-END (TIME OUT). SINCE Z13-A IS CLOCKED BY THE SAME PULSE WHICH RESETS (TRIGGERS) THE DIVIDER AND SINCE THE OUTPUT FROM Z12-C IS LOW WHEN THE TRIGGER PULSE OCCURS, Z13-A WILL BE CLOCKED LOW AND WILL STAY LOW FOR THE DURATION OF THE 12ØØ HZ SIGNAL. Z13-A REMOVES THE DISSYMMETRY FROM THE RECOVERED DATA WAVEFORM.

Z8-B BEHAVES AS A SIMPLE DIVIDE-BY-TWO WHEN THE 24ØØ HZ SIGNAL IS RECEIVED BECAUSE THE OUTPUT FROM Z12-C IS HIGH. WHEN 12ØØ HZ IS BEING RECEIVED, THE FALLING EDGE OF Z12-12 CREATES A PULSE VIA C15 AND R25 WHICH RESETS Z8-A. THIS CAUSES Z8-A TO BEHAVE AS A DIVIDE-BY-ONE (NO DIVISION) SO THE OUTPUT OF Z8-A IS THE SAME FREQUENCY (24ØØ HZ) WHEN EITHER THE 12ØØ HZ OR 24ØØ HZ SIGNAL IS RECEIVED. Z8-B ASSURES THE SIGNAL FED TO THE PHASE DETECTOR (Z7-1Ø) IS A SYMMETRICAL SQUARE WAVE.

EXCLUSIVE-OR GATE Z7-C ACTS AS A PHASE DETECTOR FOR THE PHASE LOCKED LOOP (PLL) MADE UP OF VOLTAGE CONTROLLED OSCILLATOR (VCO) Z1-A, DIVIDERS Z5, Z9-A AND RELATED COMPONENTS. THE PLL FOLLOWS THE RECOVERED CLOCK (Z8-5) AND ACTS AS FREQUENCY MULTIPLIER TO PROVIDE THE 16X CLOCK REQUIRED BY THE UART RECEIVER. THE VCO NOMINAL FREQUENCY IS 38.4 KHZ. Z5 DIVIDES THE VCO OUTPUT BY SIXTEEN. Z4-6 ACTS AS A MULTIPLEXER TO SELECT THE APPROPRIATE FREQUENCY TO DRIVE THE UART RECEIVER CLOCK DEPENDING ON THE DESIRED DATA RATE:

3ØØ	BAUD	SELECTS	THE	48ØØ	HZ	POINT	ON	THE	DIVIDER	
6ØØ	"	"	"	96ØØ	"	"	"	"	"	
12ØØ	"	"	"	192ØØ	"	"	"	"	"	
24ØØ	"	"	"	384ØØ	"	OUTPUT	FROM	THE	VCO	

THE UART RECEIVER ACCPTS DATA FROM EITHER THE RS-232 DATA TERMINAL OR THE CASSETTE DATA RECOVERY CIRCUIT DESCRIBED EARLIER. Z1Ø-A IS A 2 INPUT MULTIPLEXER USED TO SELECT DATA TERMINAL INPUT OR CASSETTE INPUT. THE DESIRED INPUT IS SELECTED BY FLIP-FLOP LATCH Z11-B WHICH IS SET OR RESET BY AN OUTPUT INSTRUCTION FROM THE PROCESSOR.

THE UART RECEIVER MAY BE CLOCKED BY THE SIGNAL DERIVED FROM THE VCO OR FROM A SIGNAL DERIVED FROM THE PROCESSOR 2MHZ OSCILLATOR. THE SELECTION IS VIA Z1Ø-B.

ALTAIR (S-1ØØ) BUS INTERFACE CIRCUIT:

THE I/O ADDRESS TO WHICH THE CI-812 WILL RESPOND IS CONTROLLED BY JUMPERS BETWEEN Z14, Z21 AND THE INPUTS OF Z2Ø. IF THE OUTPUT OF THE INVERTER IS JUMPERED TO Z2Ø, THE CI-812 WILL REACT ONLY IF THAT ADDRESS BIT IS A "ZERO". IF THE INPUT OF THE INVERTER IS JUMPERED TO Z2Ø, THE CI-812 WILL REACT ONLY IF THAT ADDRESS BIT IS A "ONE".

DURING PROPERLY ADDRESSED OUTPUT INSTRUCTIONS FROM THE PROCESSOR, DATA WILL BE STROBED INTO EITHER THE UART TRANSMITTER BUFFER (TDS) OR INTO THE CONTROL LATCHES (Z-11) DEPENDING ON THE LEVEL OF ADDRESS LINE AØ. IF AØ IS A "ZERO" THE DATA WILL BE STROBED INTO THE CONTROL LATCHES (VIA Z16-6). IF AØ IS A "ONE", THE DATA WILL BE STROBED INTO THE UART TRANSMITTER BUFFER (VIA Z16-8).

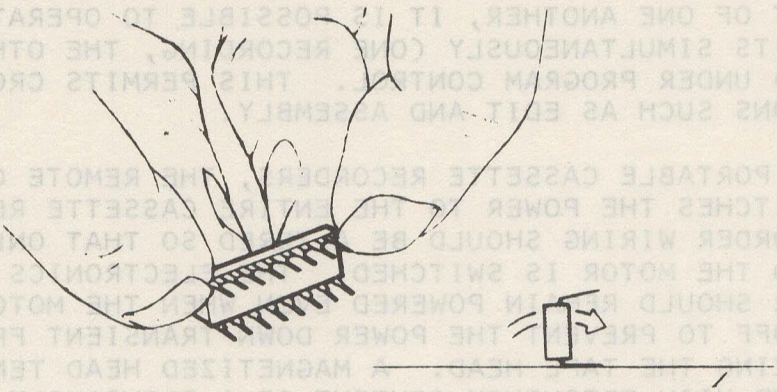
DURING PROPERLY ADDRESSED INPUT INSTRUCTIONS FROM THE PROCESSOR, EITHER THE UART STATUS OR THE RECEIVED DATA WILL BE ENABLED ONTO THE PROCESSOR INPUT DATA BUS. IF AØ IS A "ZERO", THE UART STATUS WILL BE CONNECTED TO THE PROCESSOR INPUT DATA BUS (VIA Z16-3). IT AØ IS A "ONE", THE RECEIVED DATA WILL BE CONNECTED TO THE PROCESSOR INPUT DATA BUS (VIA Z16-11). WHENEVER THE RECEIVED DATA IS READ BY THE PROCESSOR, THE DATA AVAILABLE STATUS WILL BE RESET BY Z15-11.

Z23, 24, 25 ARE 3-STATE BUFFERS WHICH INTERFACE TO THE PROCESSOR INPUT AND OUTPUT DATA BUS.

APPENDIX A

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

MOST DIP DEVICES HAVE THEIR LEADS SPREAD SO THAT THEY CAN NOT BE DROPPED STRAIGHT INTO THE BOARD. HOLD THE SIDE OF THE CHIP FIRMLY AGAINST THE FLAT SURFACE WITH BOTH HANDS, ROTATE IT A SHORT DISTANCE TOWARD ITS PINS UNTIL IT IS IN A FULL VERTICAL POSITION. THIS WILL PUT ITS BODY AT A RIGHT ANGLE TO THE ROW OF PINS. PLACE THE OTHER ROW OF PINS ON THE FLAT SURFACE AND REPEAT THE PROCESS AS ABOVE.



drawing by VectorGraphics

(1) ORIENT THE DEVICE PROPERLY. PIN 1 IS INDICATED BY A SMALL EMBOSSED DOT ON THE TOP SURFACE OF THE DEVICE AT ONE CORNER. PINS ARE NUMBERED COUNTERCLOCKWISE FROM PIN 1.

(2) INSERT THE PINS ON ONE SIDE OF THE DEVICE INTO THEIR HOLES ON THE PRINTED CIRCUIT CARD. DO NOT PRESS THE PINS ALL THE WAY IN, BUT STOP WHEN THEY ARE JUST STARTING TO EMERGE FROM THE OPPOSITE SIDE OF THE CARD.

(3) EXERT A SIDEWAYS PRESSURE ON THE PINS AT THE OTHER SIDE OF THE DEVICE BY PRESSING AGAINST THEM WHERE THEY ARE STILL WIDE BELOW THE BEND. BRING THIS ROW OF PINS INTO ALIGNMENT WITH ITS HOLES IN THE PRINTED CIRCUIT CARD AND INSERT THEM AN EQUAL DISTANCE, UNTIL THEY BEGIN TO EMERGE.

(4) PRESS THE DEVICE STRAIGHT DOWN UNTIL IT SEATS ON THE POINTS WHERE THE PINS WIDEN.

(5) TURN THE CARD OVER AND SELECT TWO PINS AT OPPOSITE CORNERS OF THE DEVICE. USING A FINGERNAIL OR A PAIR OF LONG-NOSE PLIERS, PUSH THESE PINS OUTWARDS UNTIL THEY ARE BENT AT A 45 DEGREE ANGLE TO THE SURFACE OF THE CARD. THIS WILL SECURE THE DEVICE UNTIL IT IS SOLDERED.

APPENDIX B:

REMOTE CONTROL:

MOST CASSETTE RECORDERS HAVE A REMOTE CONTROL INPUT WHICH SIMPLY TURNS THE POWER TO THE CASSETTE UNIT ON OR OFF. THIS INPUT CAN BE EASILY SWITCHED WITH A RELAY DRIVEN BY THE COMPUTER PROGRAM. THE CI-812 INCLUDES PROVISION FOR TWO DIP REED RELAYS (EXTRA COST OPTION) WHICH MAY BE CONTROLLED BY COMMANDS FROM THE PROCESSOR. SINCE THE CI-812 RECORD AND PLAYBACK CIRCUITS ARE COMPLETELY IND-EPENDENT OF ONE ANOTHER, IT IS POSSIBLE TO OPERATE TWO TAPE UNITS SIMULTANEOUSLY (ONE RECORDING, THE OTHER READING) UNDER PROGRAM CONTROL. THIS PERMITS CROSS FILE OPERATIONS SUCH AS EDIT AND ASSEMBLY.

IN MOST PORTABLE CASSETTE RECORDERS, THE REMOTE CONTROL JACK SWITCHES THE POWER TO THE ENTIRE CASSETTE RECORDER. THE RECORDER WIRING SHOULD BE ALTERED SO THAT ONLY THE POWER TO THE MOTOR IS SWITCHED. THE ELECTRONICS OF THE RECORDER SHOULD REMAIN POWERED EVEN WHEN THE MOTOR IS TURNED OFF TO PREVENT THE POWER DOWN TRANSIENT FROM MAGNETIZING THE TAPE HEAD. A MAGNETIZED HEAD TENDS TO ERASE THE HIGH FREQUENCY CONTENT OF A PREVIOUSLY RECORDED TAPE EACH TIME THE TAPE IS PLAYED.

MOST CASSETTE TAPE RECORDERS REQUIRE FROM ONE TO THREE SECONDS TO STABLIZE AFTER THE REMOTE CONTROL IS TURNED ON. CARE SHOULD BE TAKEN TO PREVENT THE 'TRASH' GENERATED DURING THIS STABILIZING PERIOD FROM CONFUSING THE COMPUTER OR ITS PROGRAM. THE FOLLOWING PROGRAMS SUGGEST HOW TO HANDLE THESE 'TRASH' INTERVALS.

TO BE QUITE FRANK, REMOTE CONTROL IS OF VERY LIMITED VALUE WHEN USED WITH THE ORDINARY CASSETTE RECORDER. YOU HAVE TO PUSH ONE OR MORE BUTTONS MANUALLY BEFORE YOU CAN BEGIN TO USE THE REMOTE INPUT. FURTHERMORE THE START UP TIME OF MOST CASSETTE RECORDERS IS SO LONG YOU WILL PROBABLY SPEND MORE TIME GENERATING AND BYPASSING INTERRECORD GAPS THAN WRITING AND READING DATA.

CAREFULLY CONSIDER YOUR INTENDED USE OF THE REMOTE CONTROL FUNCTION. IT MAY NOT BE AS WORTHWILE AS IT FIRST APPEARS.

WHEN CONTROLLING THE CASSETTE RECORDER REMOTELY, IT IS NECESSARY TO ALLOW SUFFICIENT TIME FOR THE RECORDER SPEED AND AMPLIFIERS TO STABILIZE BEFORE RECORDING OR READING DATA. THE FOLLOWING ROUTINES ILLUSTRATE SUGGESTED PRO-CEDURE.

IN THESE ROUTINES OUTPUT PORT Ø BIT Ø CONTROLS RELAY K1 WHICH SHOULD BE USED TO CONTROL THE REMOTE INPUT OF THE CASSETTE PLAYER. PORT Ø BIT 1 CONTROLS RELAY K2 WHICH IN TURN SHOULD BE USED TO CONTROL THE CASSETTE RECORDER. IF ONLY ONE CASSETTE UNIT IS USED FOR BOTH RECORD AND PLAYBACK FUNCTIONS, THE ROUTINES SHOULD BE APPROPRIATELY MODIFIED. REFER TO THE SECTION ON SOFTWARE CONSIDERATIONS.

```
:THIS PROGRAM STARTS THE RECORDER THEN WAITS
:5 SECONDS TO ALLOW THE RECORDER TO STABILIZE
:
        MVI     A,H'02'     TURN ON THE RECORDER (PORT Ø BIT 1)
        OUT     Ø
        XRA     A           SET UP 5 SEC DELAY LOOP
        MOV     B,A
        MVI     C,H'A'      ADJUST C REG TO VARY TIME
WAIT    DCR     A           THIS IS THE DELAY LOOP
        JNZ     WAIT
        DCR     B
        JNZ     WAIT
        DCR     C
        JNZ     WAIT
:
        CALL    RECORD      RECORD THE FILE
:NOW TURN OFF THE RECORDER
        XRA     A
        OUT     Ø
        RET


:THIS PROGRAM STARTS THE TAPE PLAYER THEN REQUIRES
:THAT THE FILE BE PRECEDED BY 1.5 "TRASH FREE" SECONDS
:
        MVI     A,H'01'     TURN ON THE PLAYER (PORT Ø, BIT Ø)
        OUT     Ø
RST     XRA     A           SET UP 1.5 SEC TIMEOUT
        MOV     B,A
        MOV     C,A
        IN      1           RESET DATA READY
DLY     IN      Ø           TEST FOR "TRASH"
        ANI     H'40'
        JNZ     RST         RESTART TIMEOUT IF TRASH
        DCR     C
        JNZ     DLY
        DCR     B
        JNZ     DLY
:
        CALL    READ        READ THE FILE
:NOW TURN OFF THE PLAYER
        XRA     A
        OUT     Ø
        RET
```

APPENDIX C:

'CERTIFYING' THE TAPE:

FOR BEST RESULTS A TAPE CASSETTE SHOULD BE TESTED BEFORE USE TO DETERMINE IF IT CONTAINS FLAWS WHICH WILL CREATE ERRORS. COMPUTER GRADE TAPE IS SUBJECTED TO A SERIES OF TESTS WHICH 'CERTIFY' ITS FREEDOM FROM SUCH ERROR PRODUCING FLAWS. SINCE 'CERTIFIED' CASSETTES SELL FOR TWO TO FOUR TIMES THE PRICE OF HIGH QUALITY AUDIO CASSETTES, YOU WILL PROBABLY PREFER TO TEST THE QUALITY AUDIO CASSETTES YOURSELF. THE TEST TO BE DESCRIBED IS NOT AS THOROUGH AS THE COMPUTER GRADE CERTIFICATION PROCEDURE BUT IT IS MORE THAN ADEQUATE FOR THE HOBBYIST.

THE PROCEDURE IS SIMPLY TO RECORD A CONTINUOUS SIGNAL ON TAPE THEN PLAY BACK AT REDUCED LEVEL AND LET THE CASSETTE INTERFACE WATCH FOR LOSS OF SIGNAL. IF THE TAPE PASSES THE TEST AT REDUCED PLAYBACK LEVEL IT IS ALMOST CERTAIN TO BE ADEQUATE UNDER NORMAL LEVEL CONDITIONS.

PROCEDURE:

1. RECORD A CONTINUOUS 24ØØ HZ TONE AT NORMAL OPERATING LEVEL ON THE CASSETTE. THIS CAN BE DONE BY CONNECTING THE TAPE RECORDER TO THE CI-812 CASSETTE INTERFACE SINCE THE INTERFACE GENERATES A 24ØØ HZ SIGNAL WHEN IDLE.

2. LOAD THE FOLLOWING PROGRAM INTO YOUR COMPUTER.

ADDRESS	DATA		INSTRUCTION		REMARKS
ØØØØ	3E Ø1		MVI	A, Ø1	SELECT CASSETTE INPUT
ØØØ2	D3 ØØ		OUT	Ø	
ØØØ4	DB Ø1		IN	1	CLEAR UART RECEIVER
ØØØ6	DB ØØ	LP	IN	Ø	TEST STATUS (DAV)
ØØØ8	E6 4Ø		ANI	4ØH	
ØØØA	CA Ø6 ØØ		JZ	LP	DO AGAIN IF OK
ØØØD	AF		XRA	A	TURN OFF CASSETTE
ØØØE	D3 ØØ		OUT	Ø	
ØØ1Ø			HLT		HALT THE PROCESSOR

3. CONNECT THE CASSETTE PLAYER TO THE EARPLUG INPUT OF THE CI-812.

4. REDUCE THE PLAYBACK SIGNAL LEVEL TO HALF OF THE NORMAL LEVEL.

5. START THE TAPE AND LET IT RUN FOR TWO TO THREE SECONDS.

6. NOW START THE COMPUTER EXECUTING THE ABOVE PROGRAM. AS LONG AS THERE ARE NO FLAWS IN THE TAPE THE PROGRAM WILL CONTINUE TO EXECUTE.

CERTIFICATION PROCEDURE CONT'D.

7. WHEN A FLAW IS ENCOUNTERED THE CASSETTE PLAYER WILL TURN OFF (ASSUMING THE REMOTE CONTROL OPTION IS INSTALLED) AND THE PROCESSOR WILL ENTER A HALT STATE.

EXPECT THE PROCESSOR TO HALT AT THE BEGINNING AND END OF TAPE.

MANY TIMES ERRORS ARE CAUSED BY LINT FIBERS AND DUST WHICH CAN BE REMOVED WITH TWEEZERS OR AN AIR BLAST. IF THE ERROR IS CAUSED BY A PERMANENT FLAW IN THE TAPE THE LOCATION CAN BE NOTED AND AVOIDED. THE GOOD PORTIONS OF A TAPE WITH FLAWS CAN ALSO BE RESPOOLED INTO ANOTHER CASSETTE CASE. EMPTY CASSETTE CASES ARE AVAILABLE FROM RADIO SHACK AND OTHER SOURCES.

WE HAVE HAD EXCELLENT RESULTS WITH MEMOREX MRX2 AND SCOTCH HE CASSETTE TAPE. C30 AND C45 ARE PREFERRED LENGTHS. THERE MAY BE OTHER EQUALLY SUITABLE BRANDS. CRITICALLY EXAMINE THE PRESSURE PAD OF A PROSPECTIVE CASSETTE. AN OVERSIZED PAD SUCH AS IS USED ON THE MEMOREX MRX2 IS PREFERRED FOR UNIFORM TAPE-TO-HEAD CONTACT. THE PAD SHOULD ALSO BE FREE OF LUMPS AND LOOSE LINT PARTICLES.

PLEASE NOTE

This manual has been carefully checked for accuracy, but no warranty is made as to the correctness of this document or the suitability of this product for any particular purpose. No liability is assumed for any damages, consequential or otherwise, that result from the use or misuse of this product.

WARRANTY

KIT: Defective parts will be replaced free of charge if returned to the factory within ten days of receipt of delivery or upon written statement by purchaser that the unit was unassembled or untested for some longer period due to circumstances beyond his control. Completed units returned under similar circumstances will be repaired at a labor cost of $20.00/hour, with defective parts replaced free.

THIS WARRANTY IS VOID IF THE KIT IS SOLDERED WITH CORROSIVE FLUX OR IF INTEGRATED CIRCUIT SOCKETS NOT SUPPLIED BY PERCOM ARE USED IN THE ASSEMBLY OF THIS KIT.

ASSEMBLED: Assembled units are warranted to be free from defects for ninety days from the time of shipment. If they are found to be defective in this period they may be returned to the factory for repair or replacement free of charge including return shipping.

PerCom Data Co.
4021 Windsor
Garland, Texas 75042

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PerCom Data Co.
4021 Windsor
Garland, Texas 75042

CI-812
IN-812-Ø1

JUNE 1, 1977

SUBJECT: MODIFYING THE PERCOM CI-812 FOR INVERTED AND RELOCATED STATUS BITS FOR COMPATIBILITY WITH MITS SOFTWARE.

WE HAVE HAD A NUMBER OF REQUESTS FOR INFORMATION ON MODIFYING THE PERCOM CI-812 CASSETTE/TERMINAL INTERFACE FOR INVERTED AND RELOCATED STATUS BITS.

THE PERCOM CI-812 IS CONFIGURED WITH THE UART TRANSMITTER BUFFER READY(TBMT) STATUS ON THE DATA BUS BIT 7. THE UART RECEIVER DATA AVAILABLE (DAV) IS ON THE DATA BUS BIT 6. IN BOTH CASES THE ACTIVE STATE IS HIGH. THIS CONFIGURATION WAS CHOSEN TO MAKE THE PERCOM CI-812 COMPATIBLE, INSOFAR AS POSSIBLE, WITH THE SOFTWARE AVAILABLE FROM PROCESSOR TECHNOLOGY AND IMS ASSOCIATES.

ON THE OTHER HAND, THE I/O ROUTINES WITHIN MUCH OF THE MITS (ALTAIR) SOFTWARE ASSUMES THAT THE STATUS BITS ARE INVERTED (ACTIVE STATE IS LOW) AND THAT THE RECEIVED DATA AVAILABLE IS ON DATA BUS BIT Ø.

THE FOLLOWING INSTRUCTIONS TELL HOW TO MODIFY THE PERCOM CI-812 FOR INVERTED STATUS AND TO RELOCATE THE DAV STATUS BIT TO DATA BUS BIT Ø. IF YOU WISH, PERCOM CAN PERFORM THIS MODIFICATION FOR YOU.

MATERIAL REQUIRED:

16 PIN IC SOCKET
INTEGRATED CIRCUIT 74368 OR 8Ø98
12" OF #26-#3Ø INSULATED BUS WIRE
MODEL AIRPLANE CEMENT OR EQUIV

PROCEDURE:

1. MOUNT THE 16 PIN IC SOCKET IN THE BREADBOARD AREA OF THE CI-812 ADJACENT TO THE UART (Z17).
2. CUT THE CIRCUIT TRACE GOING TO Z17 PIN 22 ON THE SOLDER SIDE OF THE CIRCUIT CARD. MAKE THE CUT SMALL SO THE CIRCUIT MAY BE EASILY RESTORED IF DESIRED AT A LATTER TIME.
3. USE INSULATED BUS WIRE TO MAKE THE FOLLOWING CONNECTIONS ON THE BACKSIDE OF THE CIRCUIT CARD. STRIP 1/8" FROM THE END OF EACH WIRE AND FORM A CIRCULAR HOOK; MAKE THE CONNECTION AND SOLDER IN PLACE BEING CAREFUL NOT TO SHORT TO ADJACENT CURCUITRY.

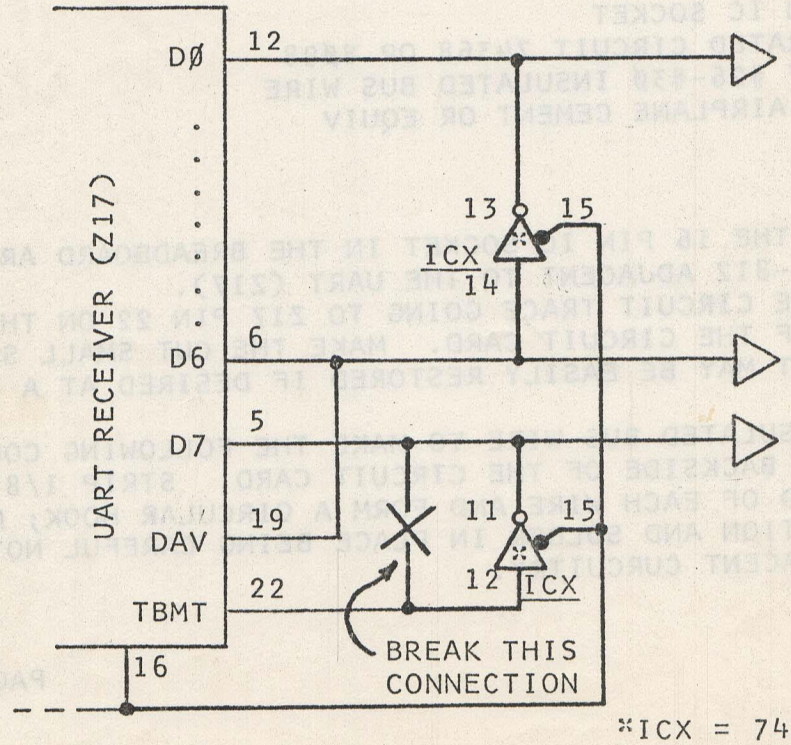
PROCEDURE CONTINUED:

( ) CONNECT ICX (THE NEW IC) PIN 16 TO Z17 PIN 1 (+5VDC)
( ) " " " 8 " " " 3 (GROUND)
( ) " " " 11 " " 5
( ) " " " 12 " " " 22
( ) " " " 13 " " " 12
( ) " " " 14 " " " 6
( ) " " " 15 " " " 16

4. RECHECK ALL CONNECTIONS. MAKE SURE THERE ARE NO SHORTS TO ADJACENT CIRCUITRY.

5. FASTEN THE WIRES TO THE CIRCUIT CARD WITH MODEL AIRPLANE CEMENT OR SIMILAR NON-CONDUCTIVE ADHESIVE.

6. PLUG THE NEW IC INTO THE SOCKET.



*ICX = 74368 (8Ø98)

LIST OF MATERIALS - PERCOM CI-812 CASSETTE/TERMINAL INTERFACE

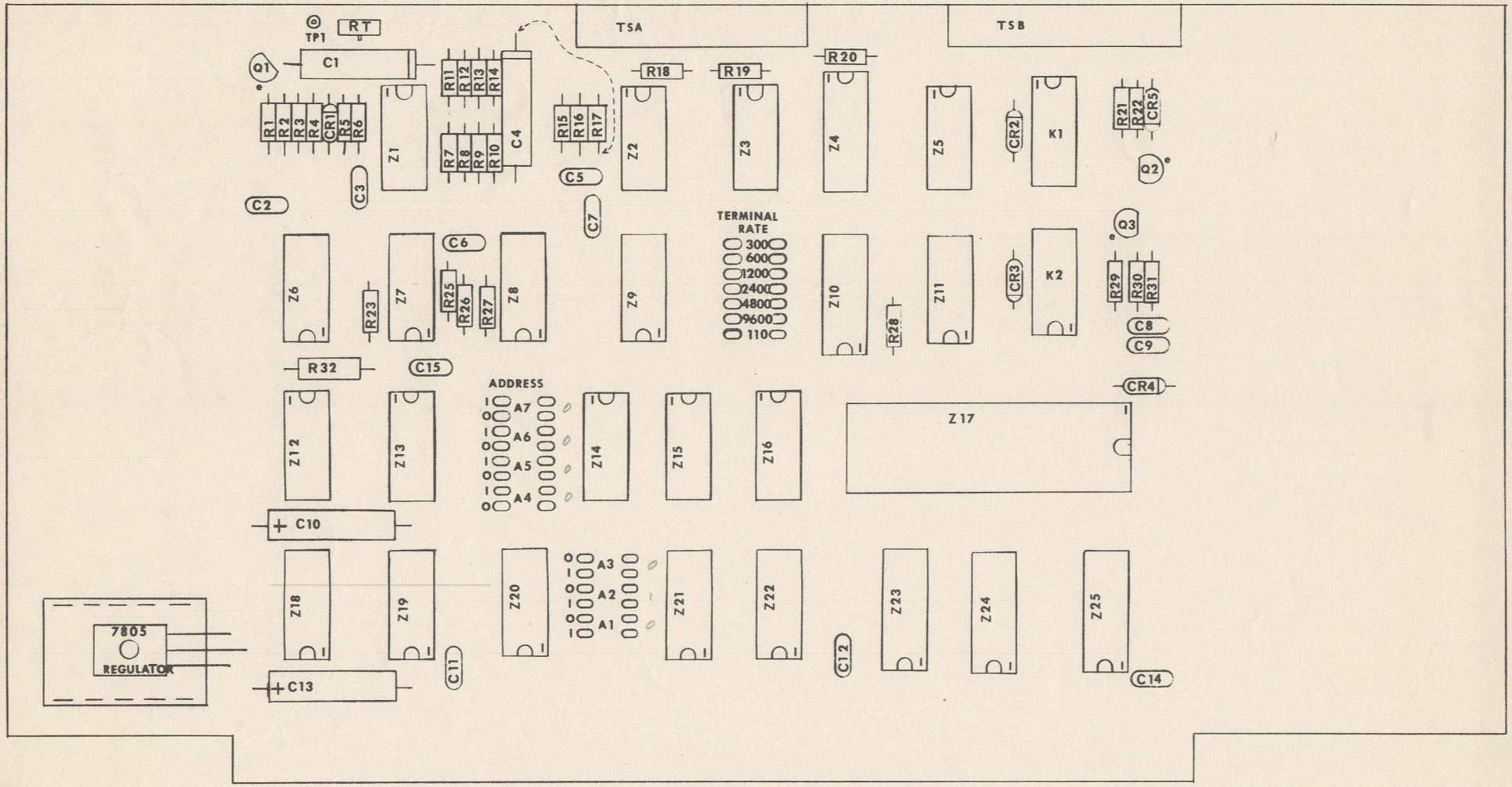
ITEM	DESCRIPTION	PART NO.	MFR.	DESIGNATOR	QTY	VENDOR	EACH	TOTAL
1	P. C. Board	CI-812			1			
2	Heat Sink 1.2"x 1"				1			
3	Screw 6-32 x 3/8"				1			
4	Nut6-32 x ¼"				1			
5	Washer #6 lock				1			
6	Integrated Circuit	74LS00N		Z15, 16	2			
7	" "	74LS02N		Z22	1			
8	" "	74LS04N		Z14, 21	2			
9	" "	74LS10N		Z12	1			
10	" "	74LS30N		Z20	1			
11	" "	74LS74N		Z8, 9, 13	3			
12	" "	7474N		Z11	1			
13	" "	74LS86N		Z7	1			
14	" "	74LS113N		Z2	1			
15	" "	74LS153N		Z4	1			
16	" "	74LS157N		Z10	1			
17	" "	74LS197N		Z3,5,6,18,19	4(5)			
18	" "	74367N (8097)		Z22,23,24	3			
19	" "	339N		Z1	1			
20	UART	2502 (AY5-1013)		Z17	1			
21	Transistor	PN3565		Q1	1			
22	"	PN5135		Q2	1			
23	"	PN5138		Q3	1			
24	Diode	IN914		CR1,5	2			
25	"	IN759A		CR4	1			
26	Regulator	7805 (LM340T-5)			1			
27	Connector	09-52-3101	Molex	TSA,B	2			
28	Resistors 180 ohm ½W CC or CF			R32	1			
29	" 100 ohm ¼w CC or CF			R21,15	~~1~~ 2			
30	" 180 "			R12,18	2			
31	" ~~470~~ "			R15	~~1~~			
32	" 820 "			R13	1			
33	" 1K "			R11,14,23,~~26~~25	4			
34	" 2.7K "			R29	1			
35	" 4.7K "			R6,16,22,31	4			

PERCOM DATA CO.

LIST OF MATERIALS - PERCOM CI-812 CASSETTE /TERMINAL INTERFACE

ITEM	DESCRIPTION	PART NO.	MFR	DESIGNATOR	QTY	VENDOR	EACH	TOTAL
36	Resistors 10K ohm ¼w CC or CF			R2,4,8,9,19,20, R27,28,30	9			
37	" 27K "			~~R25~~ R26	1			
38	" 47K "			R1,17	2			
39	" 100K "			R3,7,10	3			
40	" 68K "			R5	1			
41	Capacitors .047 uf 100v Mylar	WMF 1S47	CD	C1,4	2			
42	" 25uf 16v Elect.	500D	SPG	C10,13	2			
43	" 150 pf CM05			C3	1			
44	" 750 pf Disc	5GA	SPG	C6,15	2			
45	" .01 ufd Disc	HY-420/520	"	C2,5,7,8,9 C11,C12,C14	8			
46	Trim Pot 47K Trimmer pot.			RT	1			

PERCOM DATA CO.

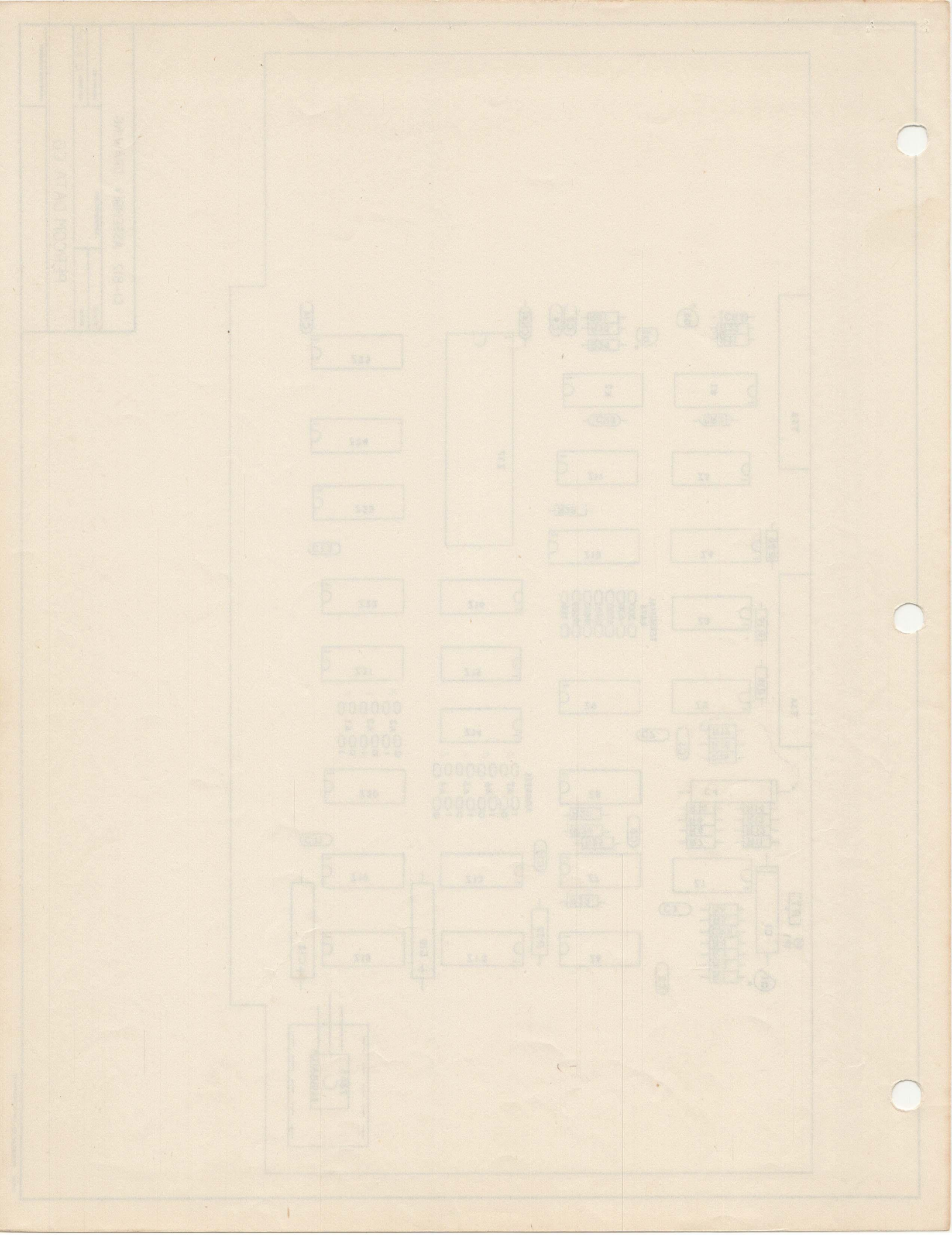


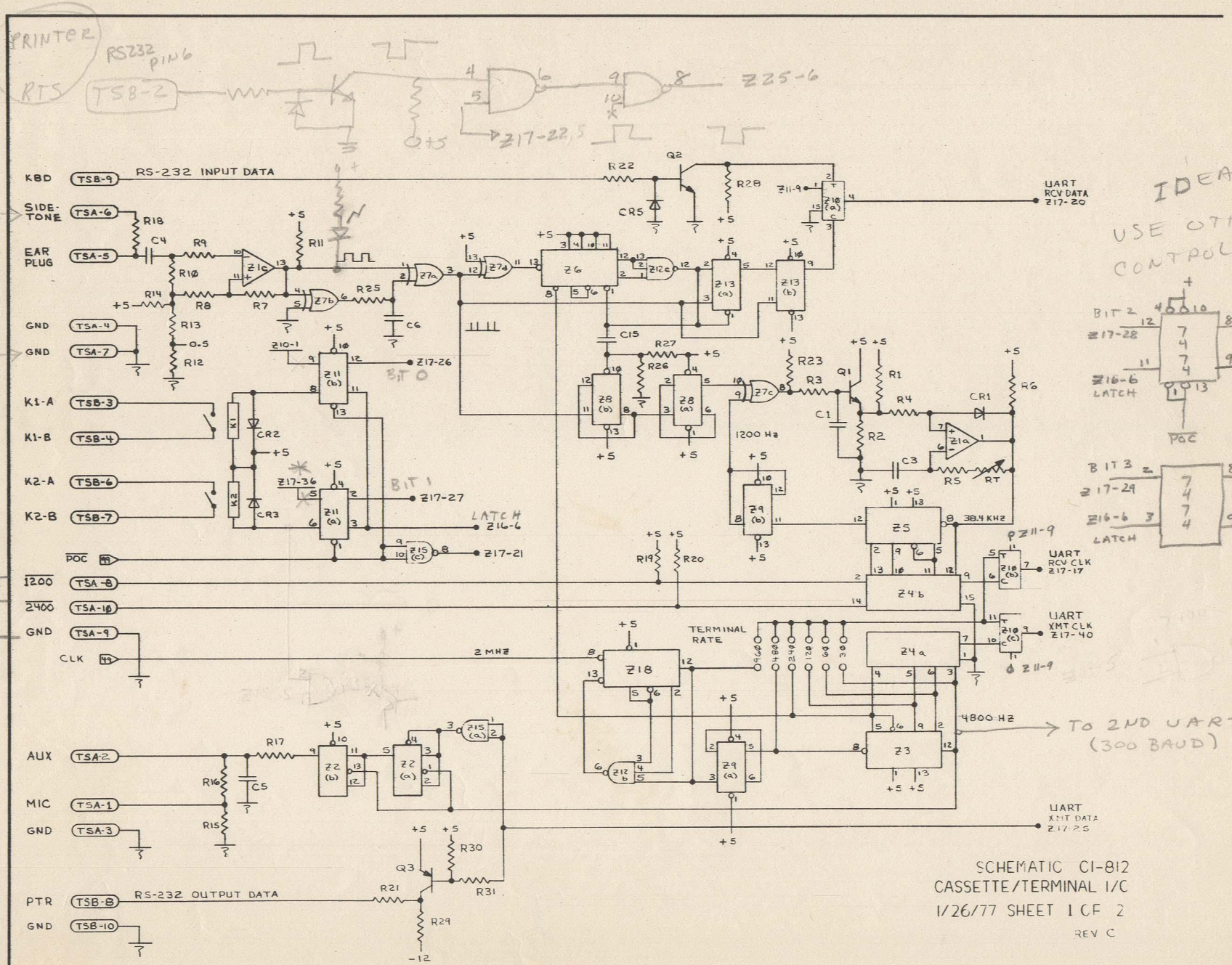
CI-812 ASSEMBLY DRAWING

SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED C 9-28-77

PERCOM DATA CO

DRAWING NUMBER





SCHEMATIC CI-812
CASSETTE/TERMINAL I/C
1/26/77 SHEET 1 OF 2
REV C

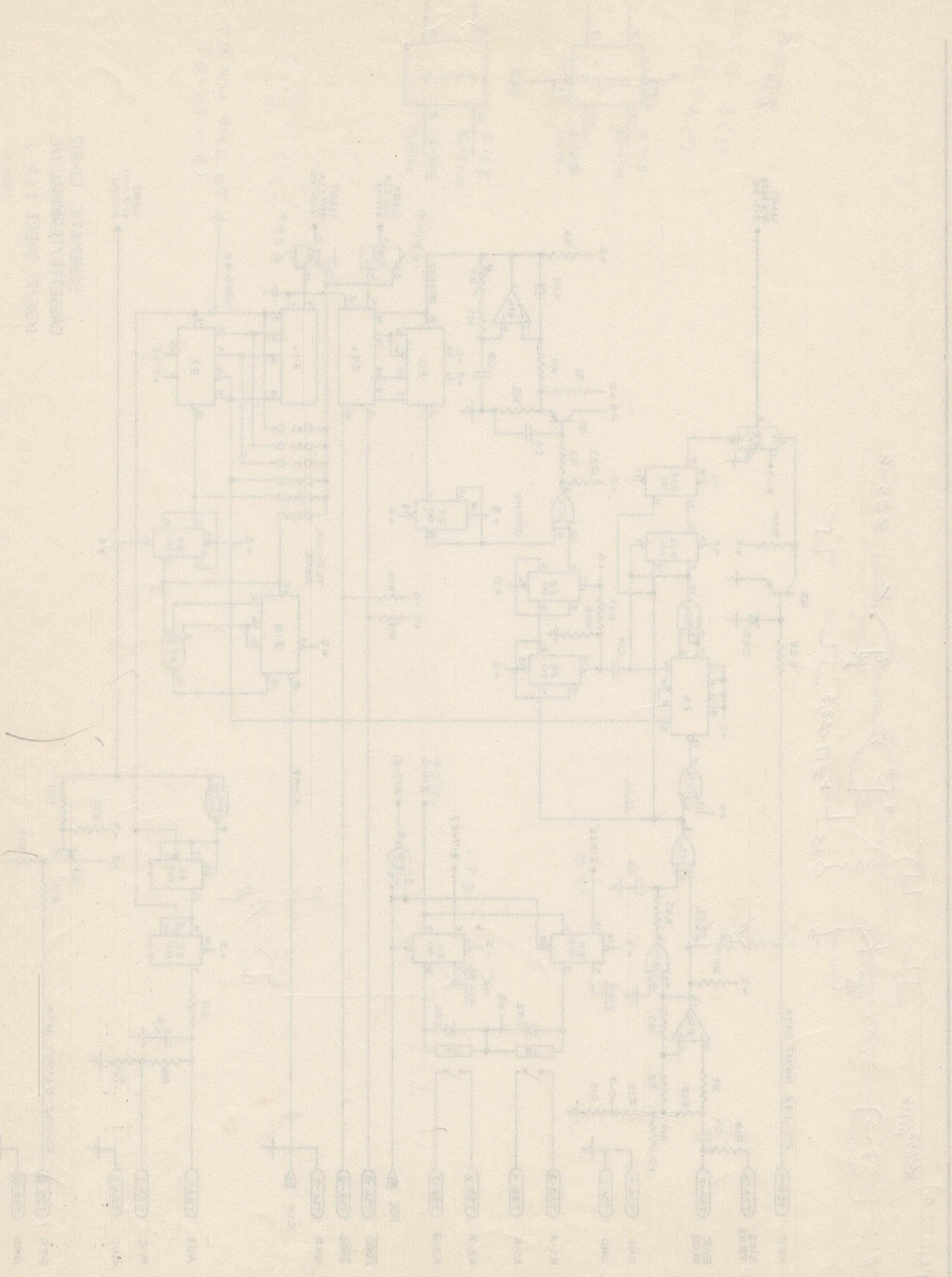
PRINTER RS232 PIN 6 RTS TSB-2 Z25-6 Z17-22,5

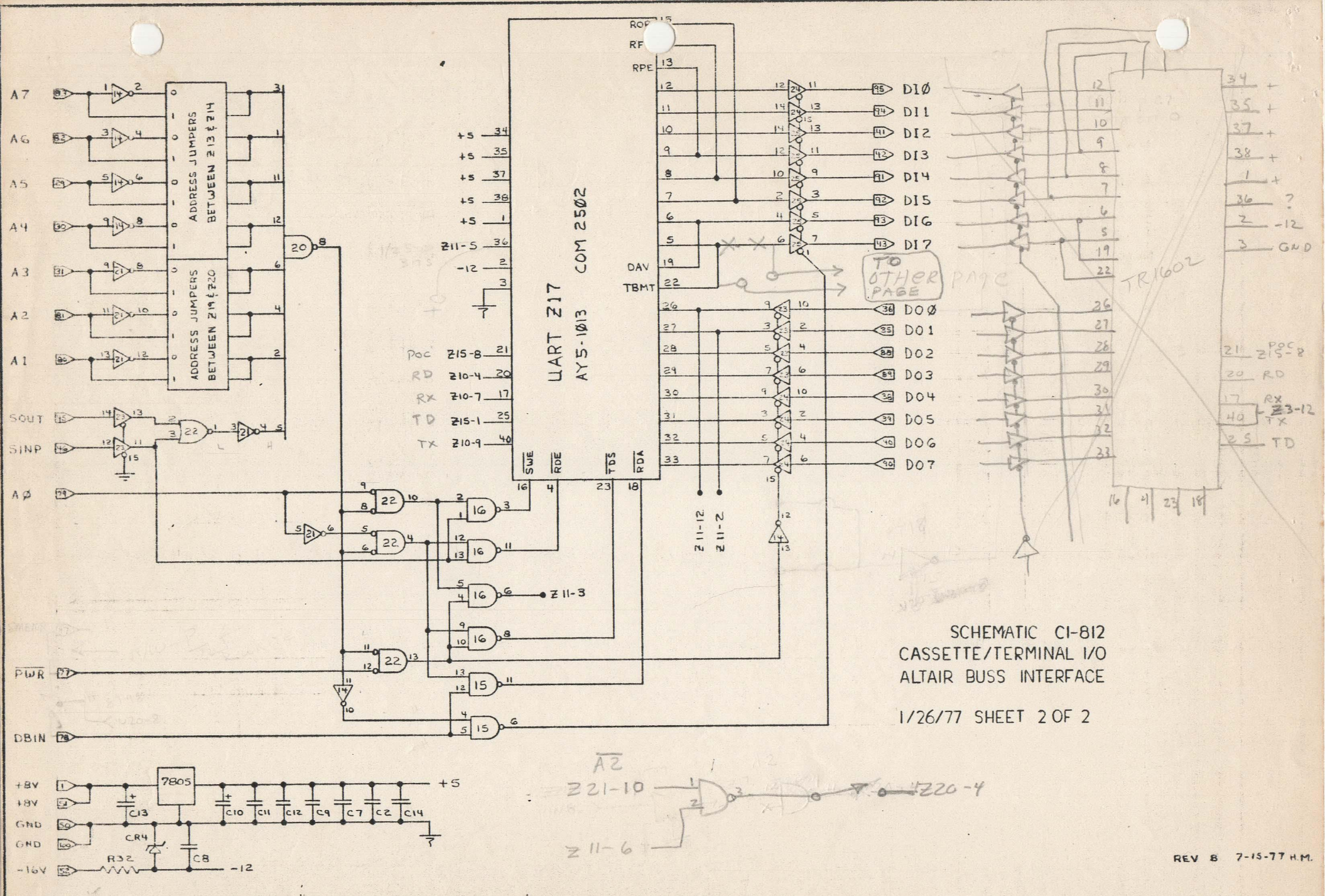
VIP PLUG KBD-3 CAS-6 CAS-5+ CAS-4+ CAS-7 CAS-8 CAS-9 CAS-10 300 CAS-2 CAS-1+ CAS-3+ KBD-2 KBD-7 VIP PLUG

IDEA! USE OTHER CONTROL BITS?

TO 2ND UART? (300 BAUD)

* This output sets 2 stop bits in UART. I gnded it at Z17-36.

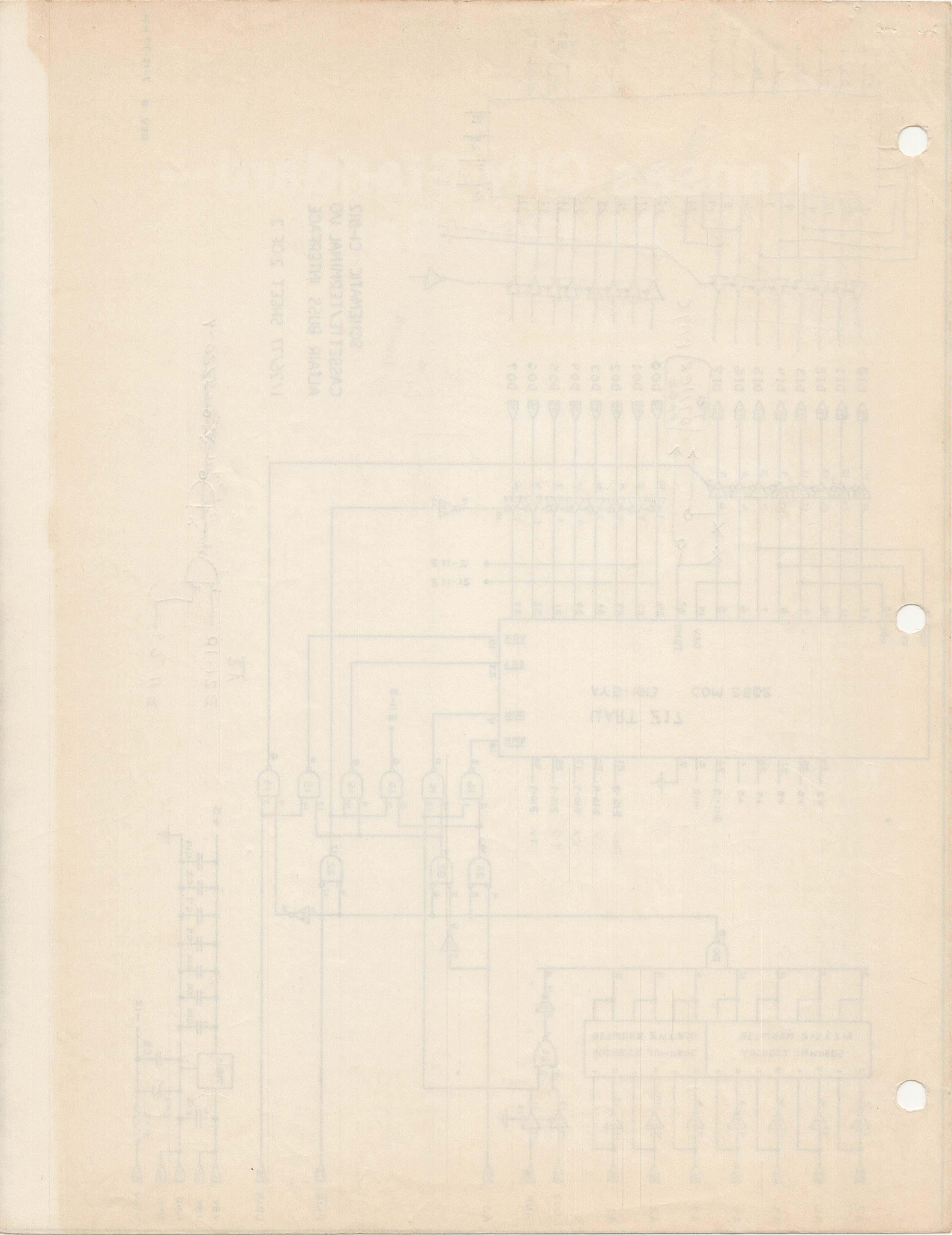




SCHEMATIC CI-812
CASSETTE/TERMINAL I/O
ALTAIR BUSS INTERFACE

1/26/77 SHEET 2 OF 2

REV B 7-15-77 H.M.



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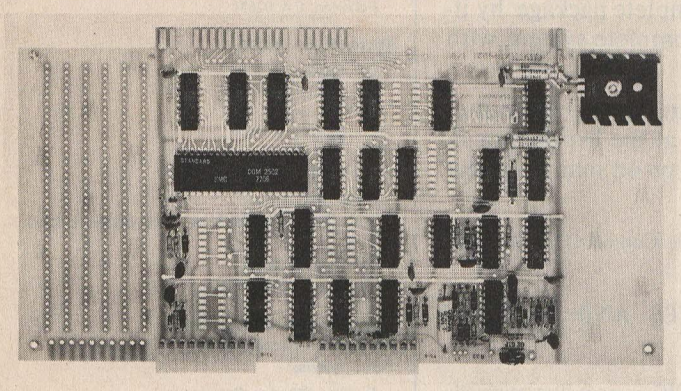
Kansas City Standard— At 1200 Baud

Although he finds some deficiencies in the CI-812 software and manual, the author is generally satistfied with Percom's I/O cassette board.



The Percom CI-812 cassette and RS-232 interface board. Strapping for the RS-232 data rate is in the center; straps to select the port address are in the lower center (A1 to A7); and the connectors for the recorder and the RS-232 device are at the top. The vacant area on the right can be used for modifications or additional features.

When I purchased the Percom CI-812 cassette and RS-232 interface board, it was my intention to write a short review of my initial experiences with it. However, in order to fit the board to my requirements, I first had to write some software. Some of the difficulties I faced and some of the solutions that I came up with should be of interest to anyone contemplating a cassette read-write interface.

I wanted to be able to read and write Kansas City Standard tapes at 300 and 1200 baud or perhaps faster. The Percom CI-812 ad struck my eye and I ordered the assembled board with remote control and test cassette (Table 1). My order arrived promptly; along with the board came a 40-page manual and a signal-level kit.

Hardware

The CI-812 is well designed and manufactured. I have had absolutely no problems with it and no component failures so far. It is made for the 8080 S-100 bus computer.

Although I purchased the assembled version, the assembly instructions were included, and I doubt anyone would have any difficulty putting it together. IC sockets are not provided or recommended by Percom unless purchased from them. The only construction required on the assembled board is the installation of the signal-level kit (a resistor and an LED) and the control and audio cables (not supplied) that go to the cassette recorder.

In addition to the cassette I/O that reads and writes tapes at 300, 600, 1200 or 2400 baud, an RS-232 compatible interface for a video terminal is provided (see "Who's Afraid of RS-232?" by Greg Pickles, *Kilobaud*, May 1977, p. 50). A simple adapter allows this to drive a 20 mil Teletype loop, also. The data rate of this interface can be strapped to 110, 300, 600, 1200, 2400, 4800, or 9600 baud. Although I haven't put the RS-232 interface to use yet, it is destined to bring my Selectric I/O to life.

Here are some of the features of the board that I particularly like:

1. Provision is made for an external monitor speaker to be connected to the board. It is nice to be able to hear what is going on when looking for trouble or trying to locate the beginning of a desired data file on the tape.

2. The signal-level kit is a joy! Start the tape, increase the volume control until the LED flickers, and you've set the playback level correctly.

3. The cassette record data rate can be set by an external switch, which I found most convenient.

4. A large area of the board is left over and can be used for modifications or additional ports as the need arises.

Factory wired, the CI-812 utilizes ports 0 and 1, but can be restrapped to use any two adjacent ports within the 8080's 256 possibilities.

I bought the remote control but found it to be of limited use. It will turn one or two recorders on or off under software control; however, this causes loss of manual control of the recorder unless I remove the remote control plug, and then I'm likely to forget to plug it back in again. Timing loops are required to allow the tape to get up to speed before reading or writing can take place. The manual quite frankly acknowledges the limitations in normal use.

Modification information is provided in case you want to interface a parallel keyboard, 110 baud Teletype or 134 baud Selectric.

My testing has shown that the average audio cassette is reliable at 300, 600 and 1200 baud, but that it takes a high-quality audio or digital tape to handle 2400 baud. A 300 baud tape can be loaded into memory and then dumped at 1200 baud to make for faster loading in the future. Keeping the original tape as insurance against accidental erasure or damage to the duplicate is a good idea.

The Manual and Test Cassette

The manual has sections on assembly, parts, schematics, modifications, theory and operation. It was written for the computer with front-panel switches and no resident operating system. The software provided consists of some test patterns at 300 and 1200 baud, a

checksum loader, and a complete micro operating system. If you have an operating system in PROM, you'd do just as well to pass up the test cassette.

The operating system has following features: examine memory, change memory, load from tape, verify tape, dump tape, and execute program. Here is how it works: Enter the bootstrap loader via the front-panel switches; this loads the checksum loader from the tape, and this, in turn, loads the operating system. The routines (Programs A, B and C) included with this article can be entered from your keyboard if your computer already has an operating system.

Address	OP Code	Assembly Language	Remarks
C9ØØ	21 ØØ ØØ	LXI ØØ ØØ	Start dump address
C9Ø3	DB Ø1	IN 1	Clear UART
C9Ø5	3E Ø3	MVI A 3	Select cassette mode
C9Ø7	D3 ØØ	OUT Ø	& set data rate
C9Ø9	DB ØØ	IN Ø	UART ready ?
C9ØB	E6 8Ø	ANI 8Ø	
C9ØD	CA Ø9 C9	JZ C9Ø9	If not loop
C91Ø	3E CB	MVI A CB	Output "CB"
C912	D3 Ø1	OUT 1	(Block start)
C914	DB ØØ	IN Ø	UART ready?
C916	E6 8Ø	ANI 8Ø	
C918	CA 14 C9	JZ C914	If not loop
C91B	7C	MOV A H	Output high order
C91C	D3 Ø1	OUT 1	address
C91E	DB ØØ	IN Ø	UART ready?
C92Ø	E6 8Ø	ANI 8Ø	
C922	CA 1E C9	JZ C9 1E	If not loop
C925	7D	MOV A L	Output low order
C926	D3 Ø1	OUT 1	address
C928	DB ØØ	IN Ø	UART ready?
C92A	E6 8Ø	ANI 8Ø	
C92C	CA 28 C9	JZ C928	If not loop
C92F	7E	MOV A M	Output data byte
C93Ø	D3 Ø1	OUT 1	pointed by H & L
C932	FE DD	CPI DD	Is it "DD"? (Block end)
C934	CA Ø3 CØ	JZ CØØ3	If so exit
C937	23	INX H	Increment address
C938	C3 28 C9	JMP C928	Get another byte

Program A. A memory-to-cassette tape dump routine. Addresses C901 and C902 will determine the location where the dump starts. If you want to start dumping at address 1A09 (hex), then enter line C900 as 21 09 1A (low-order address first). First the characters CB are placed on the tape; the start dump address is output; and then the data contained in memory is dumped until the characters DD (end block indicator) are output, at which time the routine stops and an exit to the resident operating system is made. DD should be placed in memory at the end of any program or block of data that you intend to tape.

Difficulties

I expected to read the manual once or twice, plug in the board, enter a little software and start reading and writing tapes. It didn't quite work out that way! As I've mentioned, the software in the manual and on the test cassette does not take into account the computer that already has an operating system. In addition, it is designed to be located at C000 to C1FF, which is where my monitor PROM is sitting. So I decided to write my own.

For those who use the software provided with the CI-812, here is one fault that needs correction: There are two different ways to set the output-data rate for the cassette interface. It can be the same rate as that selected by an option strap for the RS-232 interface, or it can be selected separately with an external switch. Which of these two means is actually used is controlled by software.

If the RS-232 device is a video terminal, it would normally be set too fast to clock the cassette I/O; having a switch-selectable cassette data rate is more convenient, anyway. This point is well explained in the manual, but the software still uses the RS-232 rate for the cassette I/O. Once you figure out the problem, this is easily fixed.

Lines C905 and C907 in Program A select the cassette mode and the data rate that is set by the cassette data-rate switch. If I output 02 instead of 03, then the cassette data rate is the same as that strapped for the RS-232 interface.

Software

Fortunately, enough information is given in the manual to enable you to write your own dump and load tape routines,

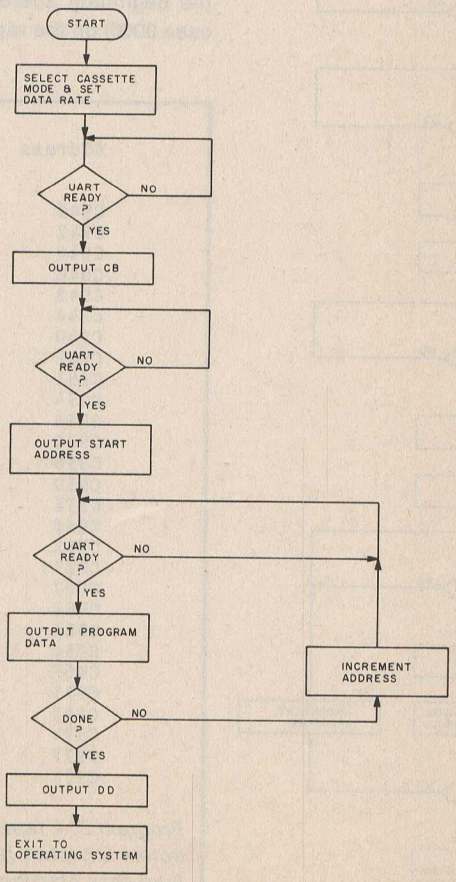


Fig. 1. Flowchart of the tape dump routine. Each symbol in the chart represents a block of assembly-language code. Compare the flowchart with the remarks in Program A to get a clearer picture.

CI-812 kit	$99.95
CI-812 assembled	129.95
IC socket kit	14.95
Remote-control kit	14.95
Test cassette	4.95

Percom Data Company
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Garland TX 75042

Table. 1.

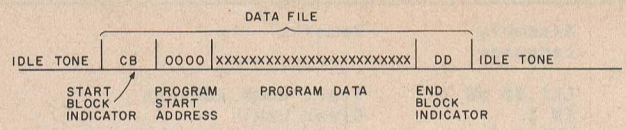

Fig. 2. A representation of how the start block indicator, program start address, program data and end block indicator appear on the tape. Before CB and after DD, the interface places a 2400 Hz idle tone on the tape. Ten to fifteen seconds of idle tone between programs on the tape makes it easier to separate them by ear with the monitor speaker.

as I did. Fig. 1 is the flowchart and Program A is the listing for my tape dump routine. The remarks column of the listing should be self-explanatory; the following information should also help.

These routines can be relocated, starting on any page boundary of memory, by replacing C9 each time it appears with the desired page number. For instance, to load these routines starting at 4000, replace C9 with 40.

Line C900 tells the routine where to find the first byte of the program that you wish to record on tape. Lines C905 and C907 select the cassette mode and set the data rate determined by the cassette data-rate switch. When the UART is ready, lines C910 and C912 record the hex characters CB on the tape. I call this my "start block indicator."

Next, C914 to C926 record the beginning address (in this case 0000) on the tape. C928 to C938 output the desired program data.

Each of my programs in memory ends with the hex characters DD. I call this my "end block indicator." When line C932 loads DD on the tape, the dump routine exits to my operating system, which gives control back to the keyboard. The data file on tape looks like Fig. 2. I chose CB and DD as my start block indicator and end block indicator, respectively, because they are not 8080-implemented operation codes and would not appear in the body of an assembly-language program.

Fig. 3 is the flowchart and Program B is the listing for my tape-load routine. C940 and C942 select the cassette mode and set the cassette data rate. (In this case, the rate is clocked by the data on the tape.) C94D, C94F and C951 keep looping until a CB is located; C95B and C95D load the high-order address byte into the H register, and C965 and C967 load the low-order address into the L register.

C96F to C978 enter the taped file into the memory pointed to by the H and L registers until DD is encountered. When this happens C974 exits to my operating system. You can write the exit in Program A and this program to any location that s... your purpose.

Fig. 4 is the flowchart of Program C, a tape-load routine intended to load tapes that do not contain CB or a load address. It normally starts with the first nonzero character but can be modified as indicated in the program caption. After being loaded with this program, a file can be dumped with Program A and then loaded with Program B from then on.

Implementation

In order to dump a program, the desired data rate is switch selected, the starting address of the program to be dumped is entered at C901 and C902, and the recorder started. After it has run for a few seconds, the command Execute (or run) C900 will record the program on tape. When the exit to the operating system is made (mine puts the cursor back on the video sc...

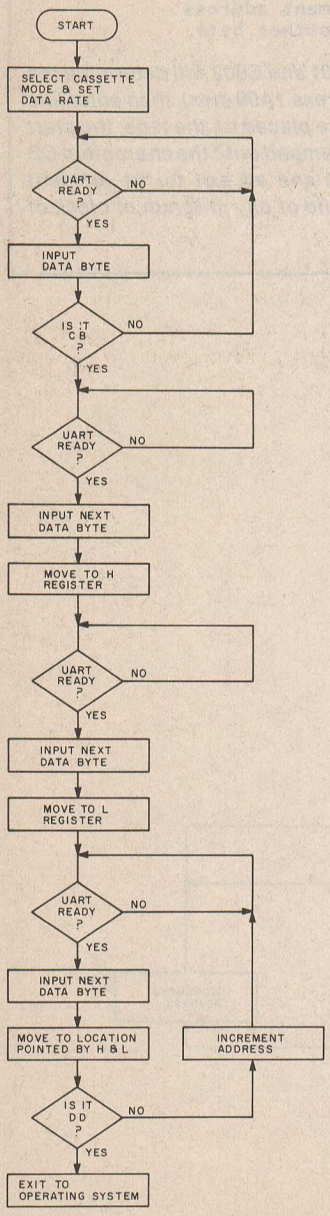

Fig. 3. Flowchart of the tape load routine listed in Program B.

Address	OP Code	Assembly Language	Remarks
C94Ø	3E Ø1	MVI A Ø1	Select cassette mode
C942	D3 ØØ	OUT Ø	& set data rate
C944	DB Ø1	IN 1	Clear UART
C946	DB ØØ	IN Ø	UART ready?
C948	E6 4Ø	ANI 4Ø	
C94A	CA 46 C9	JZ C946	If not loop
C94D	DB Ø1	IN 1	INput byte
C94F	FE CB	CPI CB	Is it CB? (start block)
C951	C2 46 C9	JNZ C946	If not loop
C954	DB ØØ	IN Ø	UART ready?
C956	E6 4Ø	ANI 4Ø	
C958	CA 54 C9	JZ C954	If not loop
C95B	DB Ø1	IN 1	Input high order address
C95D	67	MOV H A	Move to H register
C95E	DB ØØ	IN Ø	UART ready?
C96Ø	E6 4Ø	ANI 4Ø	
C962	CA 5E C9	JZ C95E	If not loop
C965	DB Ø1	IN 1	Input low order address
C967	6F	MOV L A	Move to L register
C968	DB ØØ	IN Ø	UART ready?
C96A	E6 4Ø	ANI 4Ø	
C96C	CA 68 C9	JZ C968	If not loop
C96F	DB Ø1	IN 1	Input data byte
C971	77	MOV M A	Move to memory
C972	FE DD	CPI DD	Is it DD? (end block)
C974	CA Ø3 CØ	JZ CØ Ø3	If so exit
C977	23	INX H	Increment address
C978	C3 68 C9	JMP C968	Get another byte

Program B. A tape-to-memory loading routine. This routine will read the tape until it finds the characters CB (start block indicator); it will place the next two bytes into the H and L registers; t... load data starting at the address pointed to by H and L. It will continue to load until it reads ... characters DD (end block indicator), at which time it stops reading and exits to the resident operating system.

Address	OP Code	Assembly Language	Remarks
C98Ø	21 ØØ ØØ	LXI H ØØØØ	Start load address
C983	3E Ø1	MVI A Ø1	Select cassette mode
C985	D3 ØØ	OUT Ø	& set data rate
C987	DB Ø1	IN 1	Clear UART
C989	DB ØØ	IN Ø	UART ready?
C98B	E6 4Ø	ANI 4Ø	
C98D	CA 89 C9	JZ C989	If not loop
C99Ø	DB Ø1	IN 1	Input byte
C992	FE ØØ	CPI ØØ	Is it ØØ?
C994	CA 89 C9	JZ C989	If so loop
C997	77	MOV M A	Move to memory
C998	DB ØØ	IN Ø	UART ready?
C99A	E6 4Ø	ANI 4Ø	
C99C	CA 98 C9	JZ C998	If not loop
C99F	23	INX H	Increment address
C9AØ	DB Ø1	IN 1	Input data byte
C9A2	77	MOV M A	Move to memory
C9A3	C3 98 C9	JMP C998	Get another byte

Program C. A cassette-to-memory loader intended to load tapes that do not contain CB (start block indicator) or load address. This routine will read the tape until it finds the first nonzero byte and then start loading at the address indicated in line C980. If you have a listing of the program and know the first byte to be loaded, enter that byte at C993 and change C994 to C2 (JNZ). Now the routine will read until it finds the indicated byte, and then start loading.

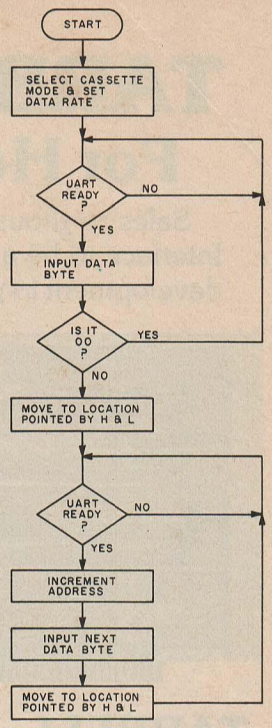

Fig. 4. Flowchart of Program C. Since the data file does not contain an end block indicator, no exit is provided for. The program is run until you hear the end of the file in the monitor speaker; then the computer is reset to end the program execution.

as an indicator), stop the tape.

When a tape is loaded with Program C, an automatic exit will not be made at the end of a file, and it is necessary to monitor the tape and push the reset button when the file has been loaded. Don't forget to write down the tape counter reading on the cassette recorder so you can find any particular file easily.

To load from tape to memory, set the data-rate switch to the rate that was used in recording, find the program on the tape if there is more than one, start the tape five to ten seconds before the beginning of the file, and command Execute C940. The routine will load all data on the tape between CB and DD into the memory locations from which it originally came.

Instead of using CB as a start block indicator for all files on a single tape, each file could have a distinctive start block indicator that would allow the load routine to find the desired file by itself. However, this is slow; it is much easier and faster to move the tape to the beginning of the file before executing the load routine.

Conclusion

Not too much has been said in this article about the RS-232 interface; not too much is said about it in the manual either. With a borrowed modem, I determined that it works properly and that I will have to develop some software in order to use it with my Selectric. I plan to pass along this information in a subsequent article.

Despite what I feel are shortcomings in the manual and software provided, I still think that the CI-812 is a good buy. It has been dependable, and, with the routines just discussed, it has given me what I was looking for when I first went shopping for a cassette interface board.■

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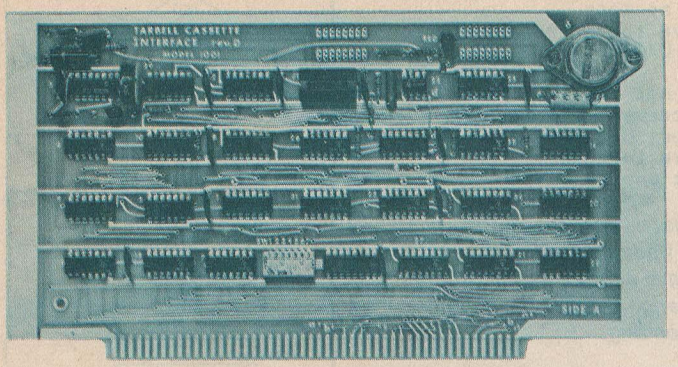

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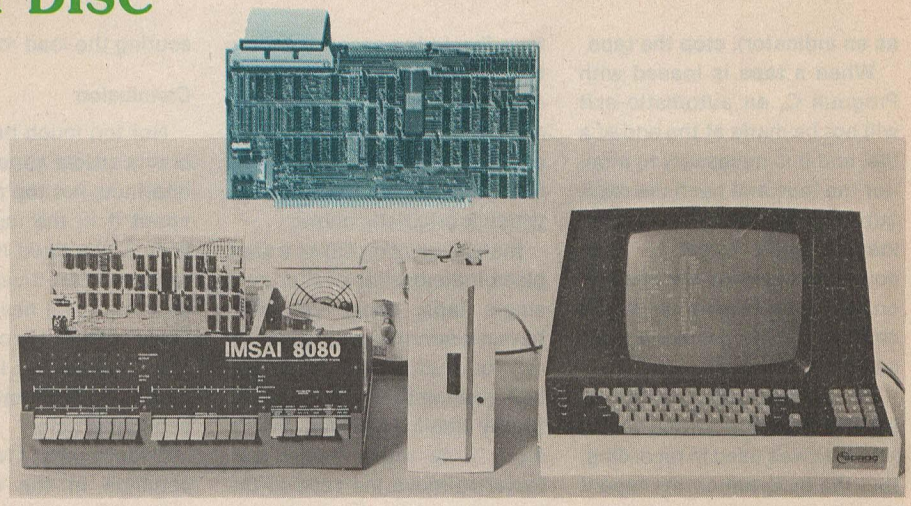
- 4 Extra Status Lines, 4 Extra Control Lines
- 37-page manual included
- Device Code Selectable by DIP-switch
- Capable of Generating Kansas City tapes also
- No modification required on audio cassette recorder
- Complete kit $120, Assembled $175, Manual $4
- Full 6 month warranty on kit and assembled units

TARBELL FLOPPY DISC INTERFACE

- Plugs directly into your IMSAI or ALTAIR* and handles up to 4 standard single drives in daisy-chain.
- Operates at standard 250K bits per second on normal disc format capacity of 256K bytes.
- Works with modified CP/M* Operating System and BASIC-E Compiler.
- Hardware includes 4 extra IC slots, built-in phantom bootstrap and on-board crystal clock. Uses WD 1771 LSI Chip.
- Full 6-month warranty and extensive documentation.
- PRICE:
  Kit $190 . . . . . Assembled $265



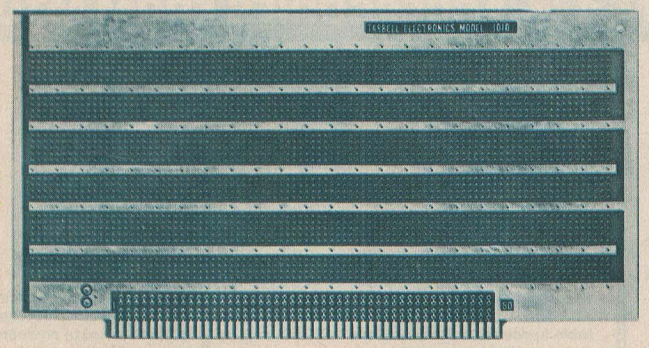
CP/M with BASIC-E and manuals: $100

Compatible Disc Drives

Ask about our disc drives priced as low as $525.

TARBELL PROTOTYPE BOARD

Model 1010



- Gold plated edge pins
- Takes 33 14-pin ICs or
- Mix 40-pin, 18-pin, 16-pin and 14-pin ICs
- Location for 5 volt regulator
- Suitable for solder and wire wrap
- ALTAIR/IMSAI compatible

Price: $28.00

For fast, off the shelf delivery, all Tarbell Electronics products may be purchased from computer store dealers across the country. Or write Tarbell Electronics direct for complete information.

*ALTAIR is a trademark/tradename of MITS, Inc.
CP/M is a trademark/tradename of Digital Research

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are being used with another BASIC language, such as Microsoft, etc., further modifications in addition to those already mentioned will be necessary. As an aid to those interested in such a conversion, I have listed the blocks of the program in Table 1; in addition, a list of the files used by the entire system may be found in Table 2. Further information on the general operation of the system may be found in Table 3.

Unfortunately, because of the size of the three programs, translating them for another BASIC may be a tough job. If you do not own CBASIC, but have the facilities to support it (CP/M, memory, etc.), consider purchasing it or CBASIC-2 as a second BASIC language. The cost is approximately $100, and CBASIC has many advantages over other BASICs. CBASIC is available for either Digital Research, Inc., or Software Systems, Inc. CBASIC-2 is available from Graham-Dorian Software Systems and probably Software Systems as well.

Although the modifications I have described are not difficult, the necessity of typing over 1000 lines of BASIC can stifle anyone's enthusiasm. As an alternative, I am willing to ship a diskette with all the programs for a nominal fee of $25. This covers the cost of a quality disk and first-class postage. (Please *do not* send diskettes, as these tend to clog the mailbox and arouse the suspicions of the neighbors.) The programs will be supplied in both ASCII text (source) and compiled form (object) on a CP/M-formatted disk.

Conclusion

Proper use of this three-part system can virtually eliminate the necessity of keeping paper files, except perhaps as a back-up. With reports A, B and D close at hand, April should be a much more pleasant month. Balancing the budget will also be easier with the help of report C. And don't forget the multitude of smaller reports the accounts-payable and accounts-receivable programs provide. With all that help you just can't lose, so let me hear from you soon, and get started computerizing your finances. ■

Digital Research, Inc.
Box 579
Garden Grove CA 93950

Software Systems, Inc.
PO Box 145
Sierra Madre CA 91024

Graham-Dorian
Software Systems
211 N. Broadway
Wichita KS 67202

✓ Reader Service—see page 179

Percom CI-812 Mod

This modification helps solve a problem that was raised in an earlier article.

Charles W. Blevins
RR3, #4 Prairie St., Box 126
Auburn IL 62615

The article by Rod Hallen in *Kilobaud*, August 1978 ("Kansas City Standard," p. 48), pointed out a problem you can encounter when using both the RS-232 interface and the cassette interface on Percom's CI-812 board: namely that it is inconvenient to require the terminal and the cassette to operate at the same data rate. Fortunately, separating the cassette and terminal interfaces is relatively simple. First, the RS-232 output is inhibited during a cassette write. Second, the UART transmitter clock frequency is set for the RS-232 rate during cassette read as well as terminal operations.

The RS-232 port is disabled by adding two NPN transistors (see Fig. 1). The bit (bit 1 of port 0) that turns on the write relay, K2, holds Q_5 off during cassette write. Thus, Q_3 is kept turned off and there is no RS-232 output. The second fix is that the transmit clock input for the UART is not routed through Z10(C) (see Fig. 2). Instead, another 74LS157 IC is added. The new 2 to 1 multiplexer is controlled by bit 1 of port 0. The terminal baud rate is fed to the UART transmit clock except during cassette write. With these fixes the UART receive clock input and data input are controlled by bit 0 of port 0, while the UART transmit clock input is controlled by bit 1 of port 0.

The effect of these changes is that the RS-232 port baud rate is independent of the cassette port. The cassette rate is selected by pins 8 and 10 on the TSA connector. The software requirements are that port 0 is set to 00 for terminal I/O, 01 for cassette read and 02 for cassette write. If port 0 is set to 03, then the cassette read/write occurs at the cassette baud rate.

In summary, cassette operations are carried out at the data rate selected by connector TSA, and terminal operations occur at the strapped terminal rate. Another advantage is that binary data tapes may be written without strange characters appearing on the terminal. ■

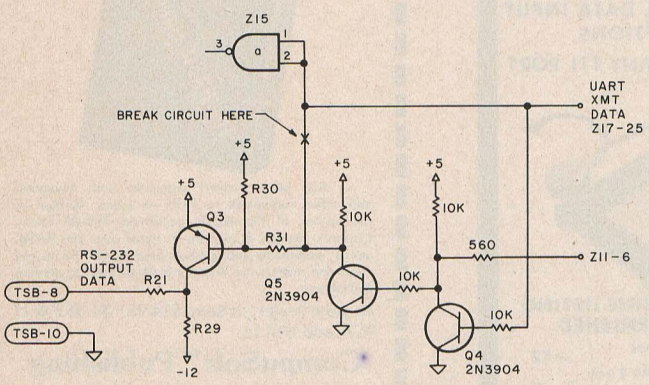


Fig. 1.

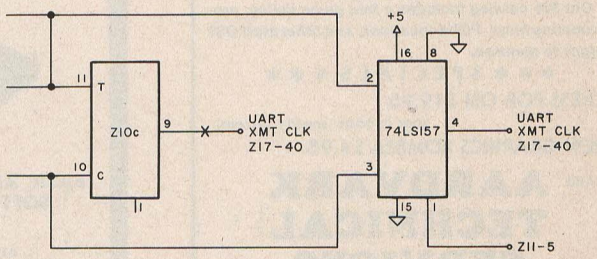
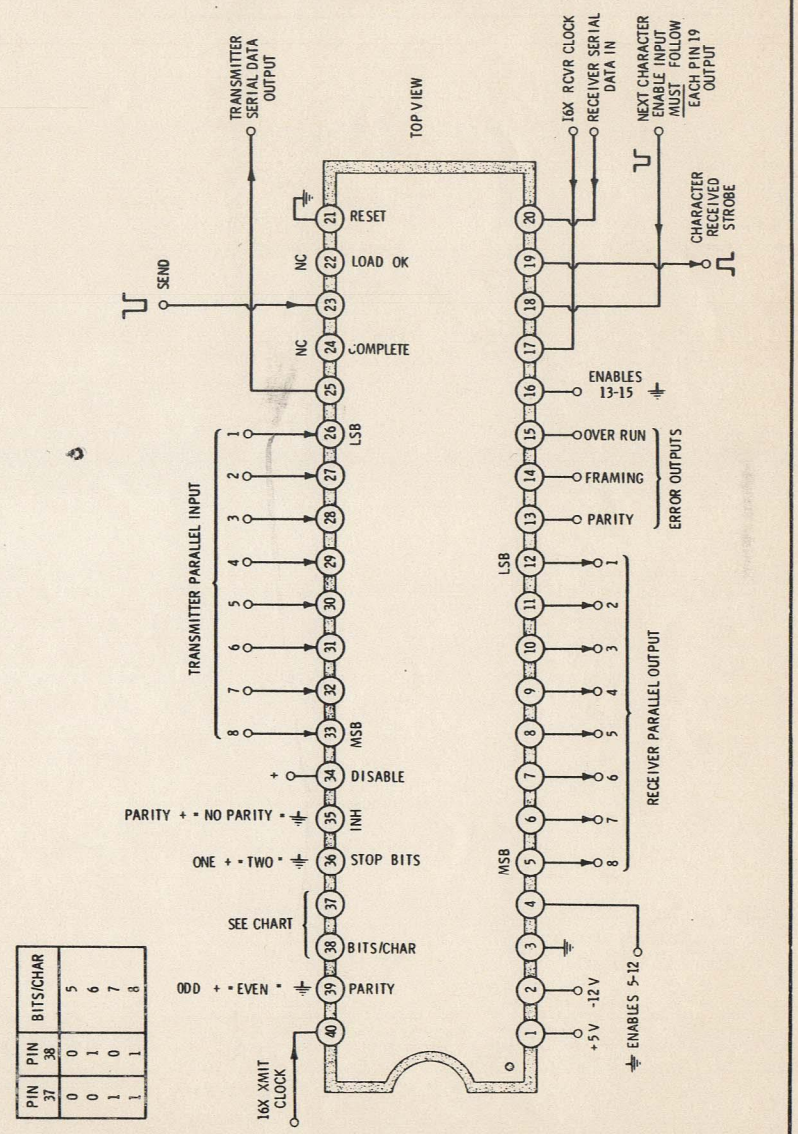


Fig. 2.

Reader Service—see page 179

1013

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)



Continued on next page

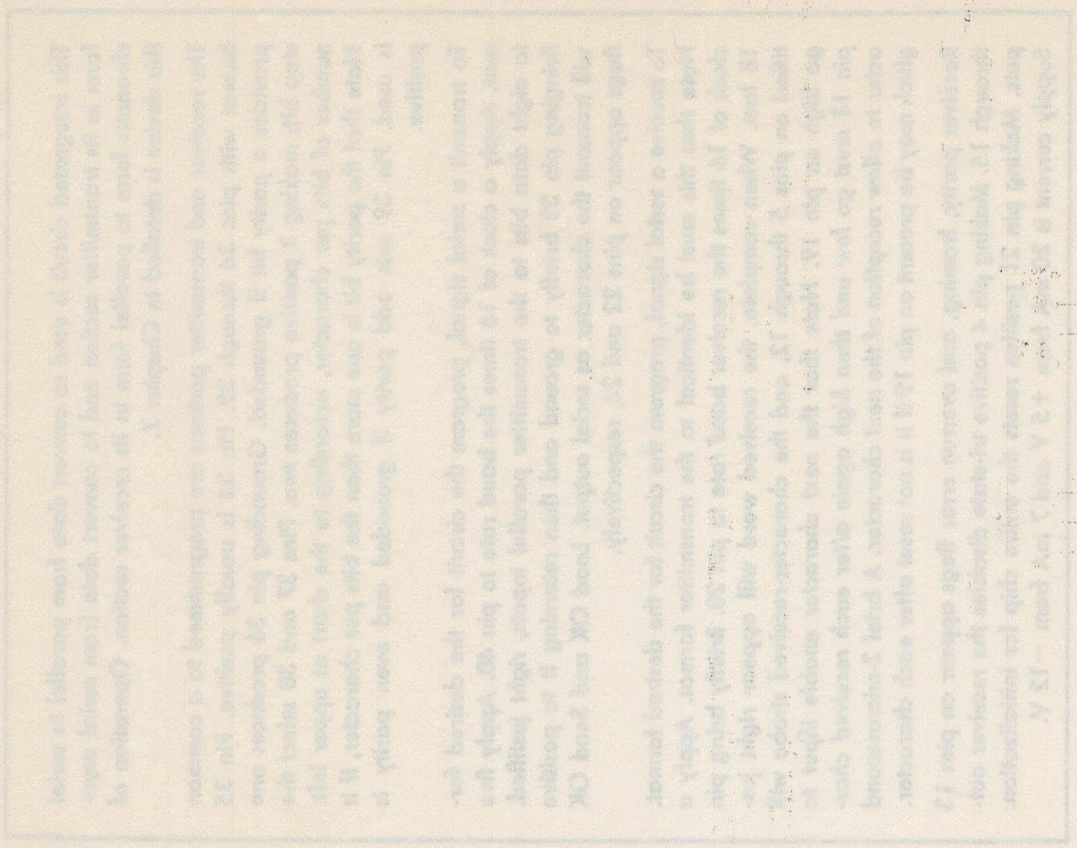
This integrated circuit is used to convert data from parallel to serial form in its *transmitter* section and to convert data from serial asynchronous form to parallel form in its *receiver* section. Operation of this device is detailed in Chapter 7.

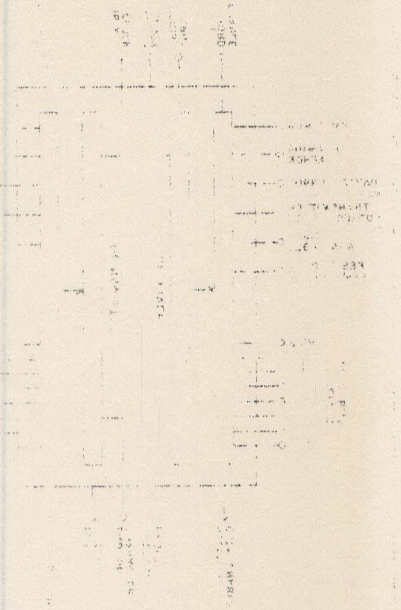
The receiver and transmitter portions are programmed to a common format with pins 34 through 39. Pin 34 is usually positive. Pin 35 provides a parity bit if grounded. Grounding pin 36 produces one stop bit; making it positive produces two. Pins 37 and 38 select the number of bits per character, according to the chart at upper left. Note that the parity bit is one more *than* the bits per character, if it is used. Pin 39 sets odd parity if grounded and even parity is positive.

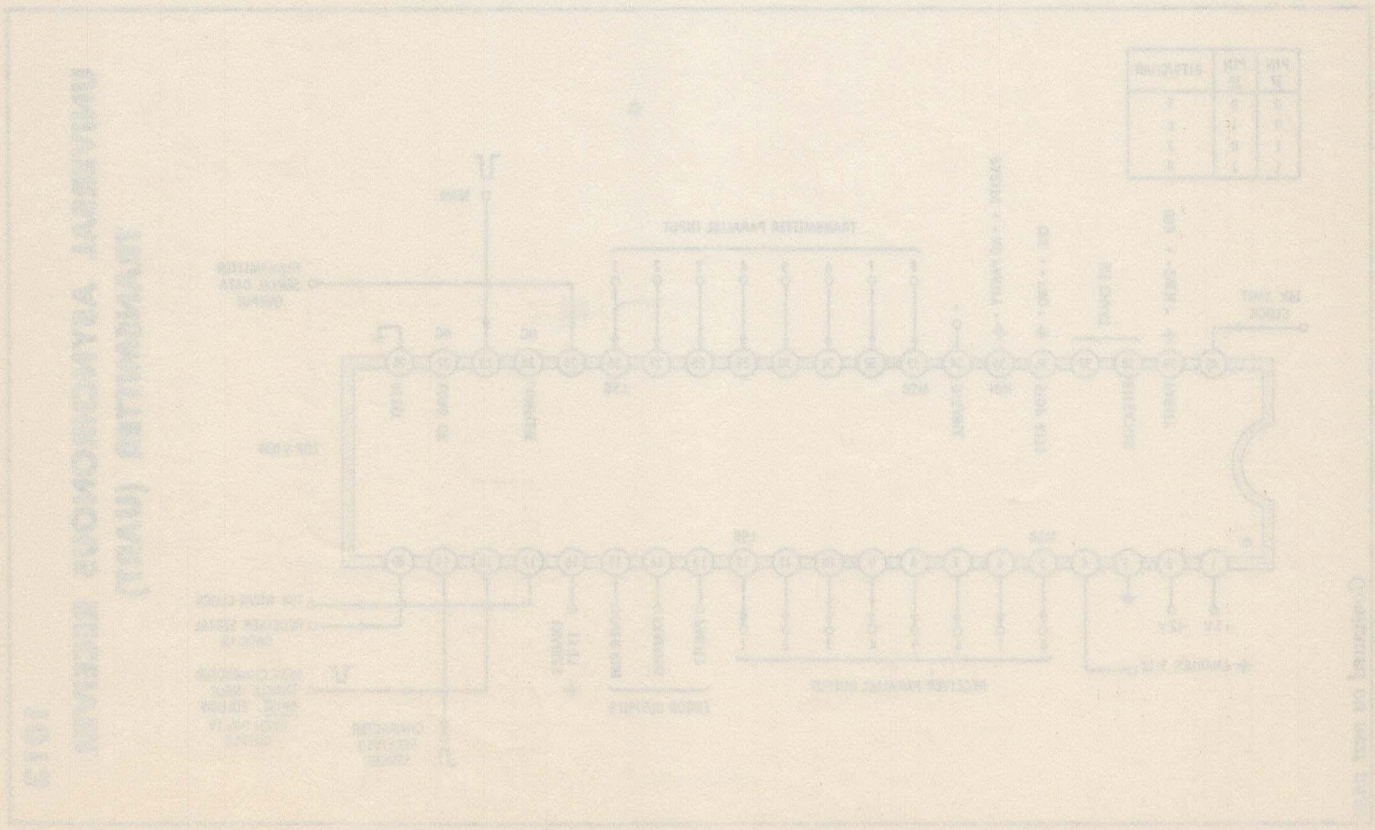
To transmit a serial signal, program the circuit for the desired format. Apply a clock of 16 times the baud rate to pin 40. Apply five to eight data bits to the transmitter parallel inputs, right justified. Bringing pin 23 briefly to ground and then returning it to positive will transmit the character as serial output. Load OK and Send OK flags appear on pins 22 and 24, respectively.

To receive a serial signal, program the circuit for the desired format. Note that this must be identical to the transmitter format. Apply a clock of 16 times the receiver baud rate to pin 20. Briefly bring pin 18 low. When complete, the received word will appear right justified on pins 5 through 12, and the character-received strobe will go high on pin 19. *Note that the next character enable input to pin 18 must go low and then high again after each received character to allow reception of the next character.* A brief 3-microsecond glitch may be present on pin 19 if it is not reset after each character.

Receiver parity, framing, and overrun error flags appear on pins 13 through 15. Making pin 4 positive tri-state disables the receiver outputs. Making pin 21 positive resets the entire chip for initialization. Supply current is 20 mA from +5 V and 7 mA from −12 V.







MARCH 1974

AY-5-1013/AY-5-1013A

UAR/T UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

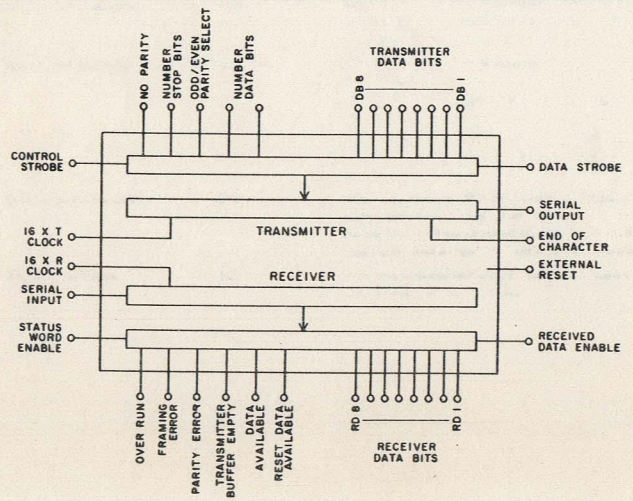
FEATURES

- DTL and TTL Compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- External reset of error flags.
- High Speed Operation—greatest through-put: 30k baud (AY-5-1013), 40k baud (AY-5-1013A).
- Tri-State Outputs—bus structure capability.
- Low Power—minimum power requirements.
- Input Protected—eliminates handling problems.
- Hermetic DIP Package—easy board insertion and mechanical handling.

GENERAL DESCRIPTION

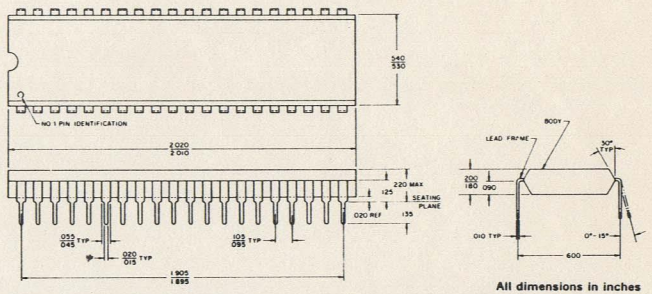
The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud rate, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL logic without the need for interfacing components and with all strobed outputs having tri-state logic.

FIGURE 1
BLOCK DIAGRAM



PIN CONFIGURATION

PACKAGE: 40 LEAD PLASTIC DUAL IN-LINE



All dimensions in inches

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	−12V Supply
3	Ground	V_{GI}	Ground
4	$\overline{\text{Received Data Enable}}$	$\overline{\text{RDE}}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{\text{RDE}}$ is "0" and a high impedance state when $\overline{\text{RDE}}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run	OR	This line goes to a logic "1" is the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	$\overline{\text{Status Word Enable}}$	$\overline{\text{SWE}}$	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{\text{Reset Data Available}}$	$\overline{\text{RDAV}}$	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available	DAV	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 13.

Pin No.	Name	Symbol	Function
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 12, 13.
21	External Reset	XR	Resets shift registers. Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "O". Clears input data buffer. Must be tied to logic "O" when not in use.
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 29, 21.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 18, 20.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 17.
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits/Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character: NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

3

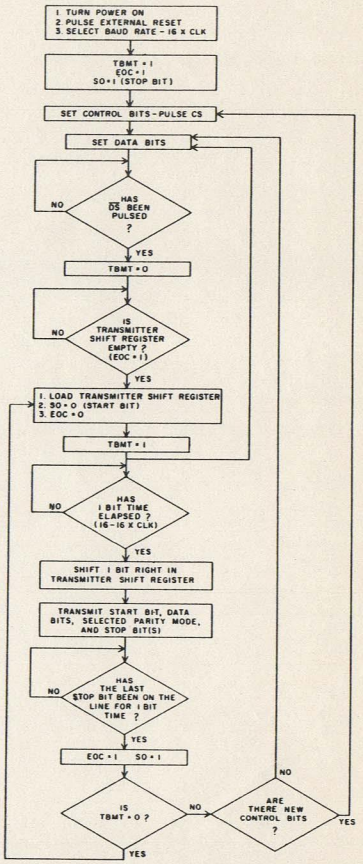
TRANSMITTER OPERATION
FIGURE 2

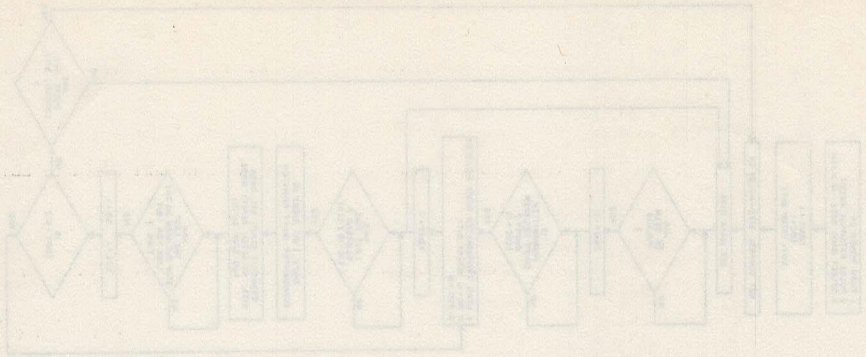
Initializing

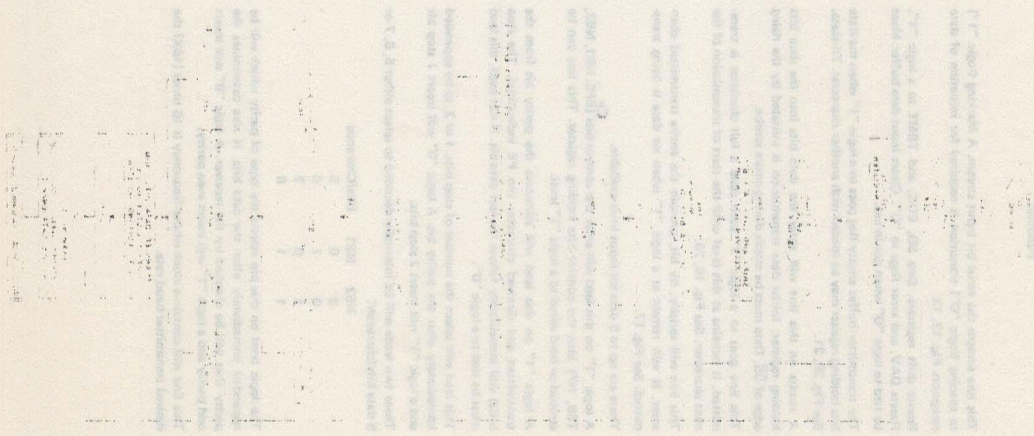
Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occuring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.







RECEIVER OPERATION
FIGURE 3

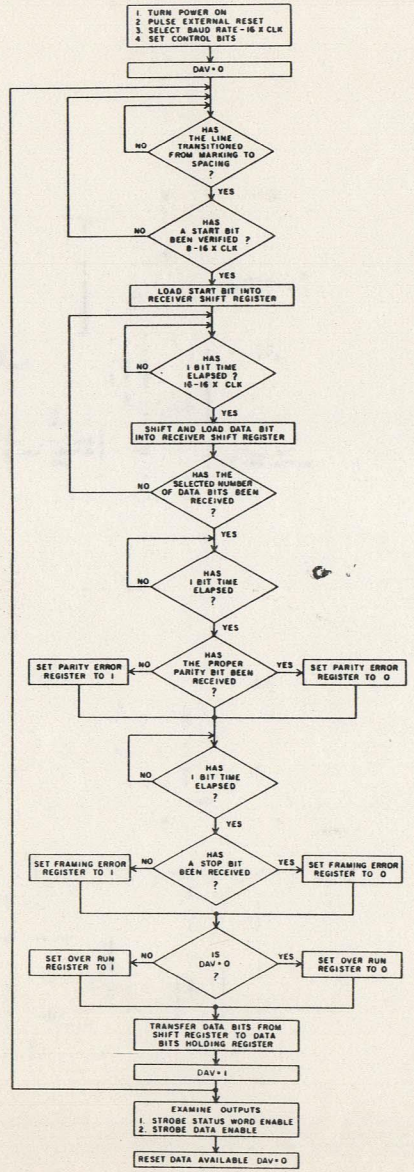
Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DAV) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{GG} (with respect to V_{CC})	−20 to +0.3V
Clock and logic input voltages (with respect to V_{CC})	−20 to +0.3V
Storage Temperature	−65°C to 150°C
Operation Temperature	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	330°

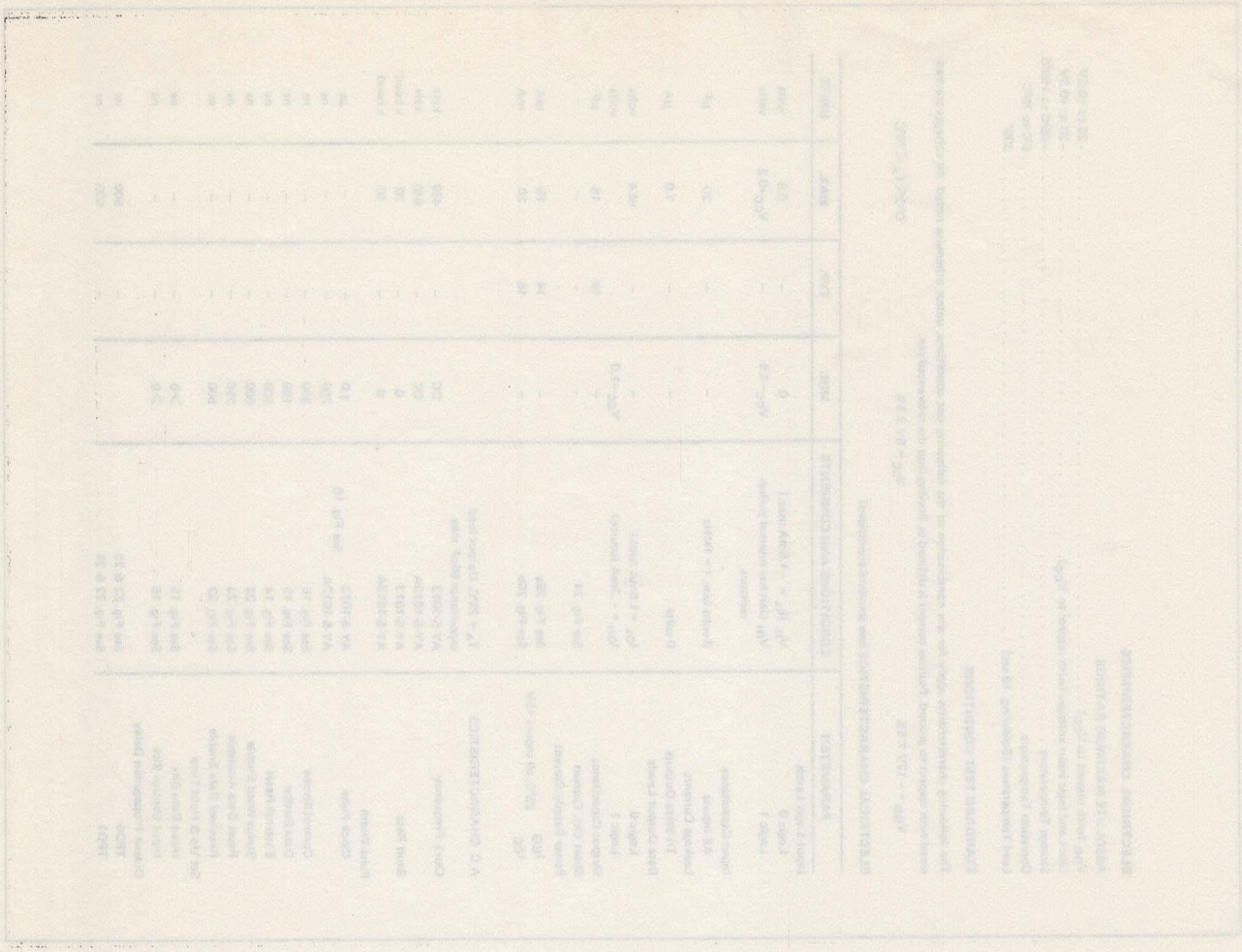
STANDARD TEST CONDITIONS

The following characteristics apply for any combination of the following test conditions, unless otherwise noted. All voltages are measured with respect to ground. Positive current is defined as flowing into the referenced pin.

$V_{GG} = -12V \pm 5\%$ $\quad V_{CC} = 5V \pm 5\%$ $\quad 0°C < T_A < 70°C$

ELECTRICAL CHARACTERISTICS (see standard conditions)

PARAMETER	CONDITIONS AND COMMENTS	MIN.	TYP.	MAX.	UNITS
Input Logic Levels					
Logic 0	V_{IL} (I_{IL} = −1.6mA max.)	0	–	0.8	volts
Logic 1	V_{IH} Unit has internal pullup resistors	V_{CC}−1.5	–	V_{CC}+0.3	volts
Input Capacitance					
All Inputs	0 volts bias, f = 1MHz	–	–	20	pF
Leakage Currents					
Tri-State Outputs	0 volts	–	–	1.0	μA
Data Output Levels					
Logic 0	I_{OL} = 1.6mA (sink)	–	–	+0.4	volts
Logic 1	I_{OH} = −.3mA (source)	V_{CC}−1.0			volts
Output Capacitance		–	10	15	pF
Short Ckt. Current	See Fig. 24	–	–	–	–
Power Supply Current					
I_{GG} 25°C, all inputs +5V	See Fig. 26a	–	14	16	mA
I_{CC}	See Fig. 26b	–	18	20	mA
A.C. CHARACTERISTICS	T_A = 25°C, Output load capacitance 50pF max.				
Clock Frequency	AY-5-1013	DC	–	480	kHz
	AY-5-1013A	DC	–	640	kHz
Baud Rate	AY-5-1013	0	–	30	k baud
	AY-5-1013A	0	–	40	k baud
Pulse Width					
Clock Pulse	AY-5-1013 See Fig. 10	1.0	–	–	μs
	AY-5-1013A	750	–	–	ns
Control Strobe	See Fig. 16	300	–	–	ns
Data Strobe	See Fig. 15	190	–	–	ns
External Reset	See Fig. 14	500	–	–	ns
Status Word Enable	See Fig. 22	500	–	–	ns
Reset Data Available	See Fig. 23	250	–	–	ns
Received Data Enable	See Fig. 22	500	–	–	ns
Set Up & Hold Time					
Input Data Bits	See Fig. 15	>0	–	–	ns
Input Control Bits	See Fig. 16	>0	–	–	ns
Output Propagation Delay					
TPD0	See Fig. 22 & 25		–	500	ns
TPD1	See Fig. 22 & 25		–	500	ns



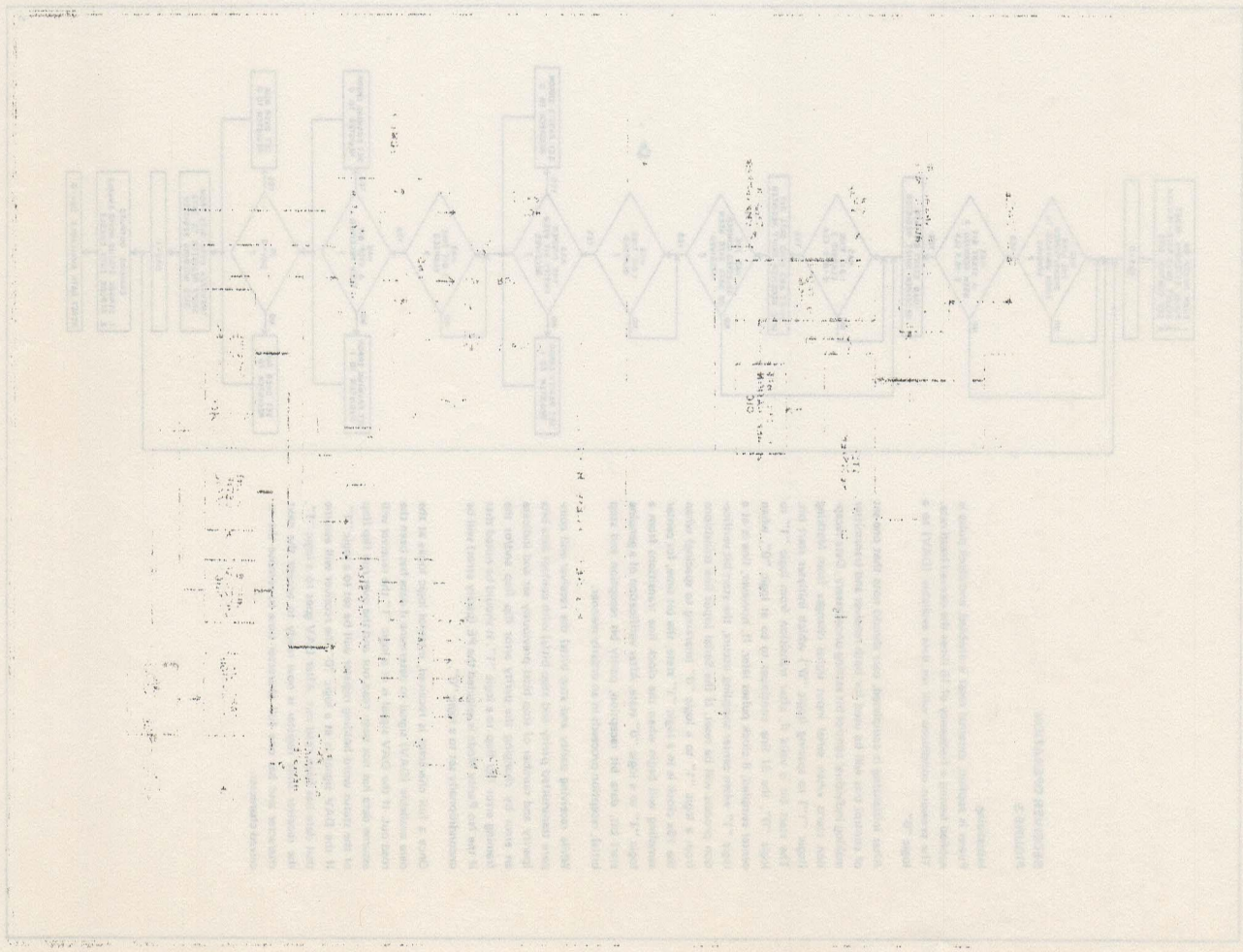


FIGURE 4 TRANSMITTER–BLOCK DIAGRAM

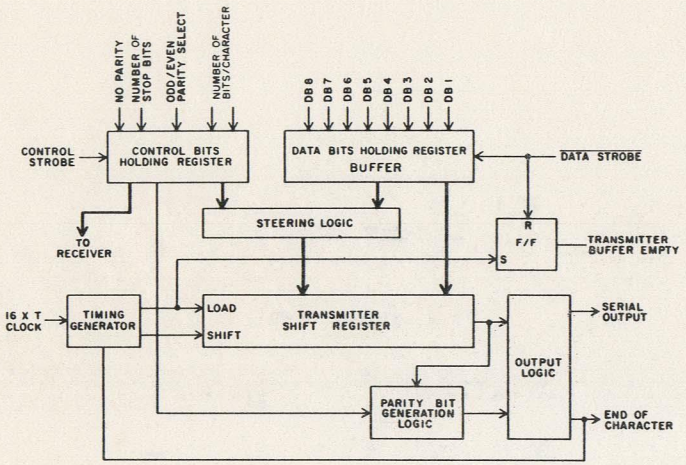


FIGURE 5 RECEIVER–BLOCK DIAGRAM

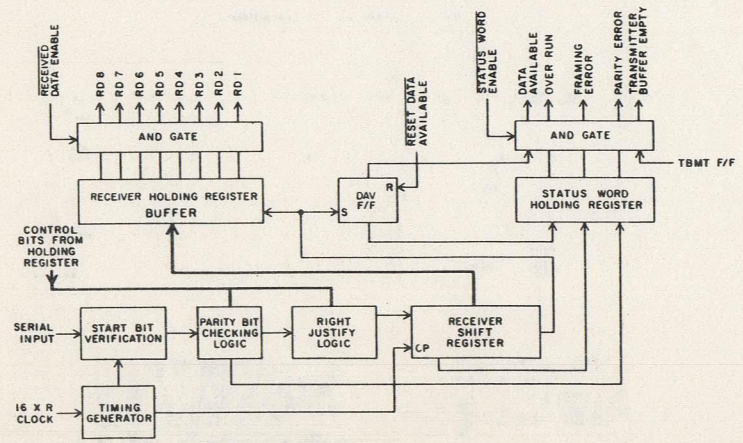
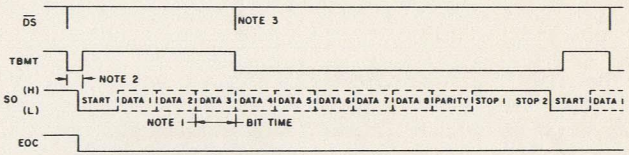


FIGURE 6 UAR/T–TRANSMITTER TIMING



NOTE: SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

DETAIL:

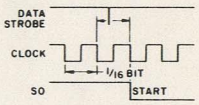


FIGURE 7 TRANSMITTER AT START BIT

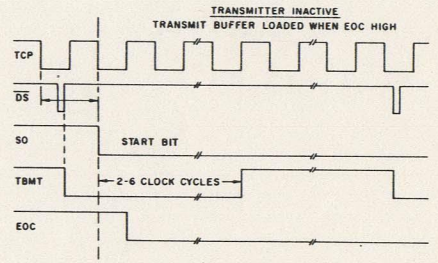
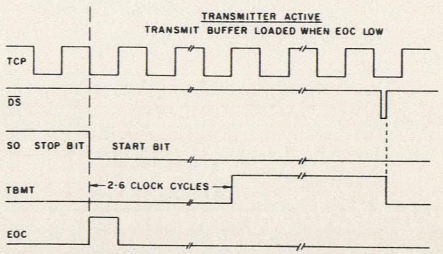
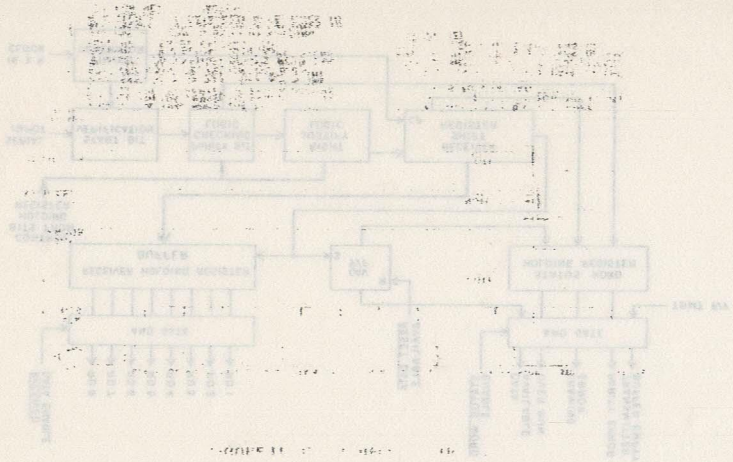


FIGURE 8 TRANSMITTER AT START BIT





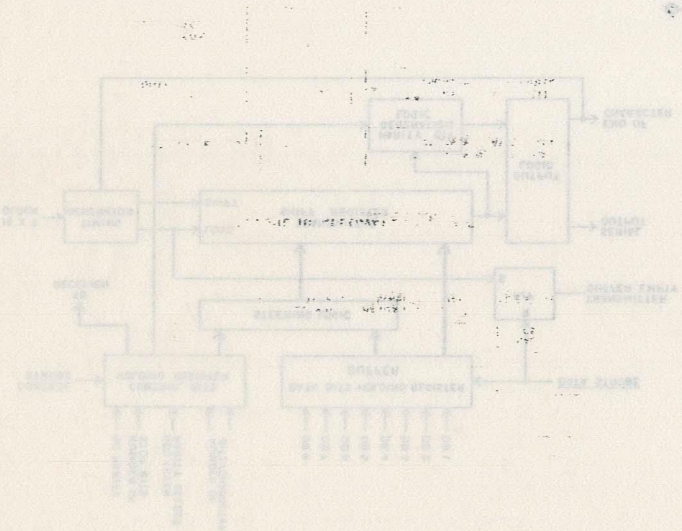
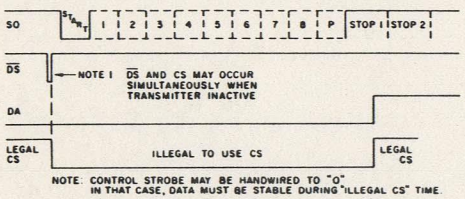
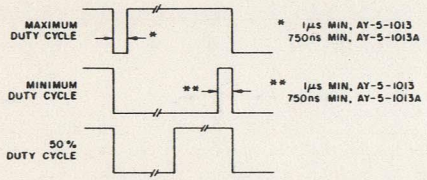


FIGURE 9 ALLOWABLE POINTS TO USE CONTROL STROBE



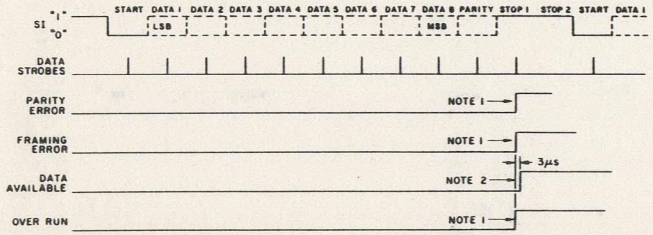
NOTE: CONTROL STROBE MAY BE HANDWIRED TO "0" IN THAT CASE, DATA MUST BE STABLE DURING "ILLEGAL CS" TIME.

FIGURE 10 ALLOWABLE TCP, RCP



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

FIGURE 11 UAR/T–RECEIVER TIMING



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE OUTPARTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RDI (PIN 12).

FIGURE 12

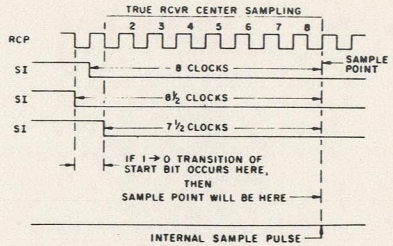


FIGURE 13 RECEIVER DURING 1st STOP BIT

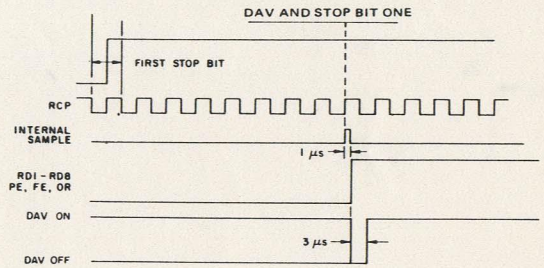
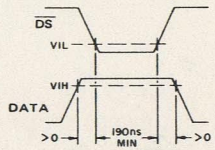


FIGURE 14 XR PULSE

WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER RECEIVED DATA SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV.

FIGURE 15 $\overline{DS}$



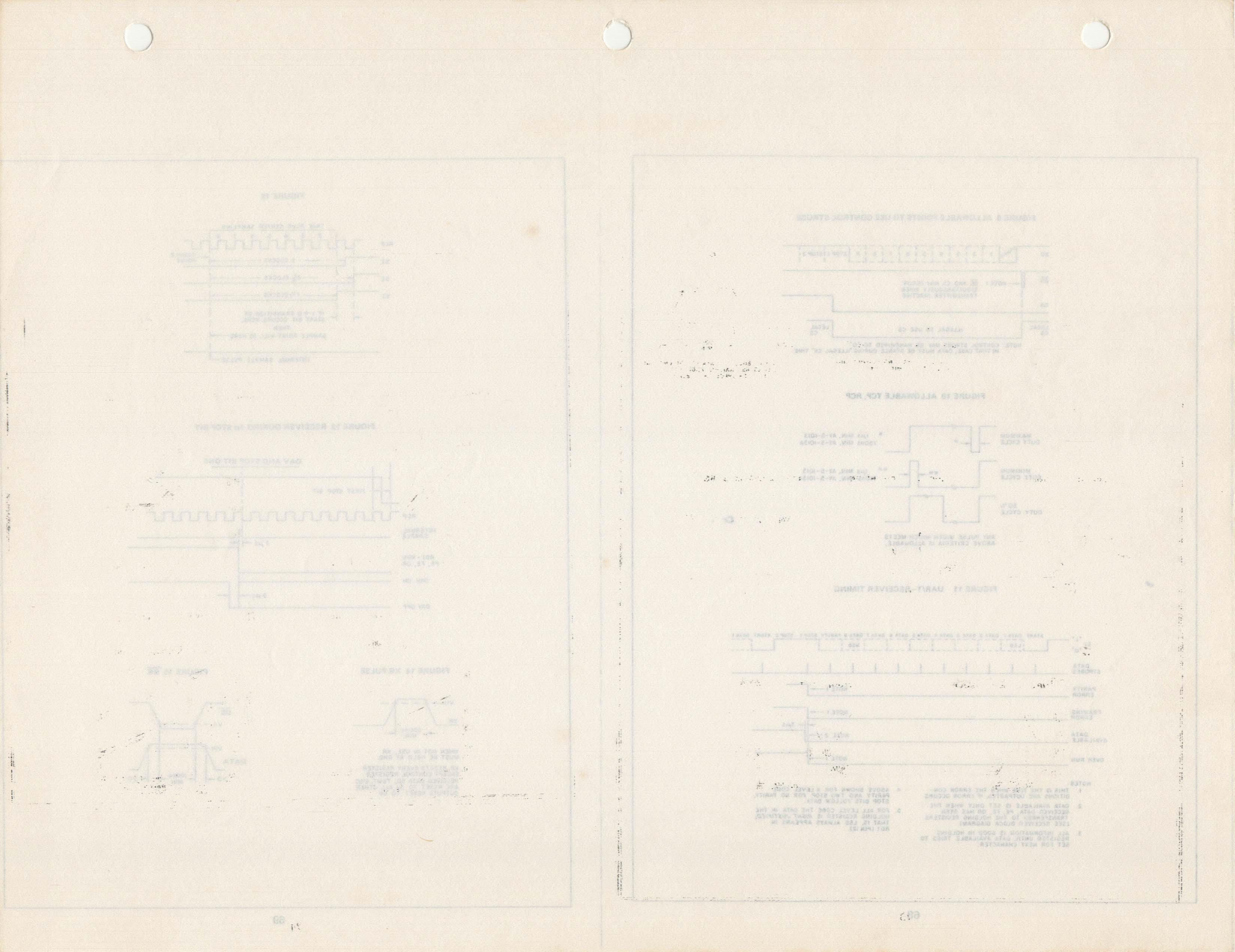
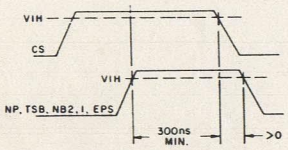
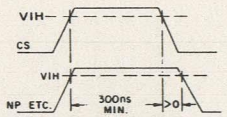


FIGURE 16a CS



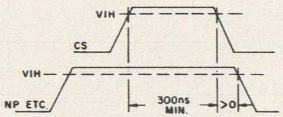
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

FIGURE 16b



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM.

FIGURE 16c



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

FIGURE 17 SEROUT

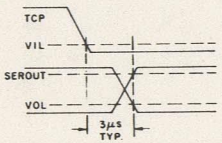


FIGURE 18 EOC TURN-ON

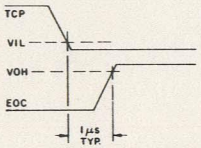


FIGURE 19 TBMT TURN-OFF

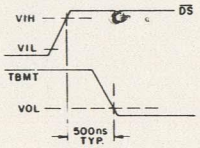


FIGURE 20 EOC TURN-OFF

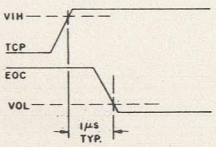


FIGURE 21 TBMT TURN-ON

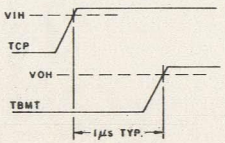


FIGURE 22 $\overline{RDE}$, $\overline{SWE}$

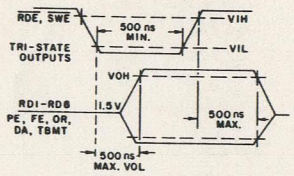


FIGURE 23 $\overline{RDAV}$

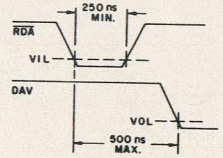


FIGURE 24 SHORT CIRCUIT OUTPUT CURRENT

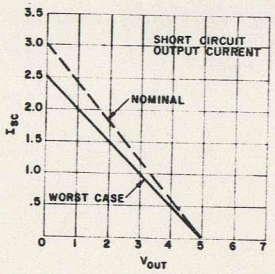


FIGURE 25 RD1–RD8, PE, FE, OR, TBMT, DAV

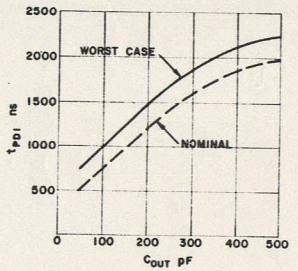


FIGURE 26a –12 VOLT SUPPLY CURRENT

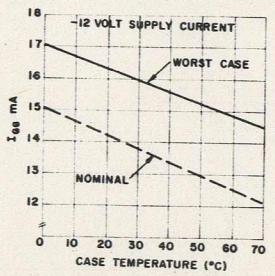


FIGURE 26b +5 VOLT SUPPLY CURRENT