Short-Form Specification

The STD 32 Bus Specification

A Brief Overview

The *STD 32 Bus Specification* extends the capabilities of the STD-80 Series standard, while remaining compatible with existing STD Bus cards. These excerpts from the specification provide mechanical and electrical details pertinent to a technical evaluation of the bus. For the complete specification, contact the STD 32 Manufacturers Group.

Mechanical

Connectors

The 136-pin STD 32 card connector uses cantilever beam construction with a hemispherical contact point. This connector/contact style is similar to PC and Micro Channel designs, and is considered one of the most reliable in the industry (see **Figure 1**).

Connector Specifications

- *Number of Contacts:* 136
- *Contact Design:*
  Cantilever beam, hemispherical contact point
- *Contact Plating:*
  30 microinches of gold over 50 microinches nickel (minimum)
- *Current Capacity:*
  1.0 Amp (minimum per pin)
- *Mating PCB Thickness:*
  0.062 inch ±0.007 inch
- *Operating Temperature:*
  -40° to +85° C
- *Mating Cycles: 500 (minimum)*

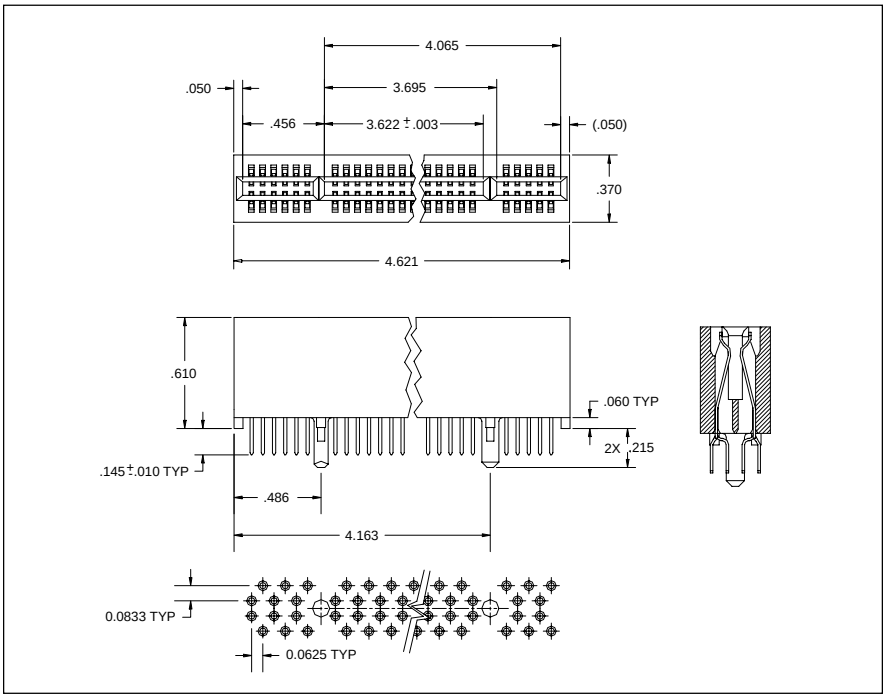

Figure 1. *The STD 32 connector contacts are arranged as 68 directly opposed pairs. The center section of 57 contact pairs provide backward compatibility with older STD-style cards and expansion to 16-bit non-multiplexed transfers. The remaining 11 contact pairs on the card extensions allow 32-bit non-multiplexed data transfers while maintaining compatibility with older 8-bit STD I/O cards.*

- *Insertion Force:*
  6 ounces per contact pair
- *Vibration:*
  10 Hz to 2 KHz at 15 Gs with 0.06-inch displacement
- *Contact Normal Force:*
  135 grams per contact
- *Connector Body:*
  Glass-filled polyphenylene sulfide, UL 94V-0
- *Insulation Resistance:*
  Greater than 50,000 Megohms
- *Operating Humidity:*
  0 to 95% with no condensation

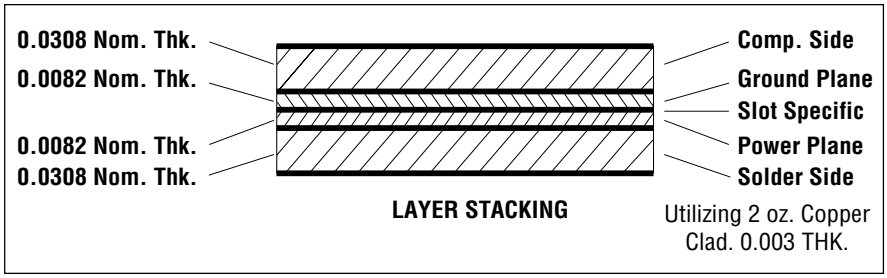

Figure 2. *Backplane signal impedance is enhanced by maximizing the separation of the signal planes from the power and ground planes. Minimizing the trace width and maximizing its height also enhances impedance.*

Connector Mating Surfaces

The design of the connector mating surface (or "gold fingers") is the core of the *STD 32 Bus Specification*. This design not only allows the number of contacts to increase from 56 to 136 but also provides a backward-compatible platform for the thousands of older STD I/O cards currently available for the STD Bus.

Mating Surface Specifications

- *PCB Thickness:*
  0.062 Inch ±0.007 inch
- *Plating:*
  30 microinches of gold over 50 microinches of nickel
- *Design:*
  Conforms to STD 32 P/E finger dimensions

Backplane

Another critical component in an STD 32 system is the backplane. The backplane design incorporates several important features including increased backplane signal impedance.

A higher backplane signal impedance means "cleaner" signals are sent across the backplane. That is, ringing and reflections are minimized. This is especially important during signal transitions between the TTL threshold regions of 0.8v and 2.0v (see **Figure 2**).

Backplane Specifications

- *Minimum Center-to-Center Trace Spacing: 16 mil*
- *Minimum Trace Width: 8 mil*
- *Number of Copper Planes:* 5 maximum
- *Unloaded Impedance:* 55 ohms (minimum)
- *Copper Clad Thickness: 2 oz.*
- *Backplane PCB Thickness:* 0.093-inch (minimum)

Electrical

Pin Descriptions

See **Figures 3** and **4**.

Clock Frequency

The STD 32 Bus uses the signal CLOCK* for synchronous communication between Bus Masters (CPUs) and peripheral boards, and for other system management features such as arbitration. The Permanent Master is responsible for driving CLOCK* in all systems. The CLOCK* frequency is 8 MHz.

Transfer Types

STD 32 defines five classes of backplane transfers for communication between Bus Masters and peripherals. Standard Architecture (SA) transfers define compatible cycles for older STD-80 Series peripherals. Both 8- and 16-bit SA transfers are allowed through dynamic bus sizing. Extended Architecture (EA) transfers support 8-, 16-, and 32-bit data widths with a transfer cycle as short as one CLOCK* cycle. The maximum bandwidth for EA transfers is 32 Mbytes/second (see **Figure 5**). The cycle performed is dynamically sensed by the Bus Master from control signals that the peripheral returns. The default cycle is an SA 8-bit (SA8) cycle to remain compatible with older technology cards designed around the STD-80 Series specification.

Address Space

STD 32 supports a full 32-bit address space for memory cycles and a full 16-bit address space for I/O cycles. Older boards that do not decode the full I/O address range are allowed if they decode the IOEXP signal. IOEXP is driven low by STD 32 CPU boards in the I/O range FC00h to FFFFh, and high for all other addresses.

This mechanism prevents I/O boards that decode less than 16 bits and IOEXP low from being redundantly mapped throughout the I/O space. All STD 32 I/O boards must decode the full 16-bit address space. STD 32 memory boards must decode 24 bits of address for SA cycles and 32 bits of address for EA cycles.

Standard Architecture (SA) Cycles

SA cycles are nominally five CLOCK* cycles. The upper 8 bits of memory address (A16 to A23) is multiplexed with the data lines to allow the full, 16 Mbyte address range required by 286 and 386SX processors. This multiplexing scheme is compatible with STD-80 Series boards. 8-bit data transfers are performed unless the memory board being accessed returns MEM16* at the beginning of the cycle. When MEM16* is returned, a 16-bit SA cycle is defined (SA16), and the additional data signals D8 to D15 are driven on non-multiplexed pins. I/O cycles can also be 16 bits if the signal IO16* is driven by the I/O board during the transfer.

Extended Architecture (EA) Cycles

STD 32's default transfer is an SA class cycle. If, during the beginning of a cycle, EX8*, EX16*, or EX32* is driven low by a peripheral board, then Extended Architecture cycles are performed. EX8*, EX16*, and EX32* define 8-, 16-, and 32-bit EA transfer capability, respectively. Burst cycles are also possible for EA devices when the peripheral drives

COMPONENT SIDE			
Pin	**Mnemonic**	**Signal Flow**	**Description**
1	+5VDC	In	Logic Power
3	GND	In	Logic Ground
5	VBAT	Bidir	Battery Power
7	A19/D3	Out/Bidir	Address/Data
9	A18/D2	Out/Bidr	Address/Data
11	A17/D1	Out/Bidr	Address/Data
13	A16/D0	Out/Bidr	Address/Data
15	A7	Out	Address
17	A6	Out	Address
19	A5	Out	Address
21	A4	Out	Address
23	A3	Out	Address
25	A2	Out	Address
27	A1	Out	Address
29	A0	Out	Address
31	WR*	Out	Write Mem or I/O
33	IORQ*	Out	I/O Address Select
35	IOEXP	Out	I/O Expansion
37	INTRQ1*	In	Interrupt Request 1
39	STATUS1*	Out	CPU Status 1
41	BUSAK*	Out	Bus Acknowledge
43	INTAK*	Out	Interrupt Acknowledge
45	WAITRQ*	In	Wait Request
47	SYSRESET*	Out	System Request
49	CLOCK*	Out	Clock
51	PCO	Out	Priority Chain Out
53	AUX GND	In	AUX Ground (bussed)
55	AUX +V	In	AUX Positive (+12VDC)

CIRCUIT SIDE			
Pin	**Mnemonic**	**Signal Flow**	**Description**
2	+5VDC	In	Logic Power
4	GND	In	Logic Ground
6	DCPDN*	Bidir	DC Power Down
8	A23/D7	Out/Bidir	Address/Data
10	A22/D6	Out/Bidr	Address/Data
12	A21/D5	Out/Bidr	Address/Data
14	A20/D4	Out/Bidr	Address/Data
16	A15	Out	Address
18	A14	Out	Address
20	A13	Out	Address
22	A12	Out	Address
24	A11	Out	Address
26	A10	Out	Address
28	A9	Out	Address
30	A8	Out	Address
32	RD*	Out	Read Mem or I/O
34	MEMRQ*	Out	Mem Address Select
36	BHE*	Out	Byte High Enable
38	ALE*	Out	Address Latch Enable
40	STATUS0*	Out	CPU Status 0
42	BUSRQ*	In	Bus Request
44	INTRQ*	In	Interrupt Request
46	NMIRQ*	In	Non-Maskable Int Request
48	PBRESET*	In	Push-Button Reset
50	CNTRL*	Bidir	Aux Timing
52	PCI	In	Priority Chain In
54	AUX GND	In	AUX Ground (bussed)
56	AUX -V	In	AUX Negative (-12VDC)

Notes: An asterisk (*) indicates a low level active signal. Address lines A16 to A23 are multiplexed on data lines D0 to D7 on each address cycle for STD-80 compatibility. PCO and PCI are not typically used on peripheral cards. All boards not supporting PCO and PCI should tie these two signals together.

Figure 3. *This table illustrates the STD 32 Bus P Pinouts (Table 3-2 in the STD 32 specification). See the next page for a description of the E Pinouts.*

SLBURST*, while the Bus Master is driving MSBURST*. Burst cycles allow up to 32 bits of data to be transferred on every CLOCK*, for a 32 Mbyte/second transfer rate. The nominal cycle (non-burst) is a two-CLOCK* cycle. EA cycles use separate data and address signals (not multiplexed) to allow pipelined execution of the transfer.

Direct Memory Access (DMA)

Backplane Direct Memory Access (DMA) transfers are also defined for the Extended Architecture, at up to 32 Mbytes/second. Each of the first 15 slots in an STD 32 card cage has a dedicated set of DMA control signals to allow for true backplane DMA transfers. Older technology DMA mechanisms on the STD bus have required front plane cabling.

Interrupt Topology

STD 32 defines five bused interrupt signals and one slot-specific interrupt for application use and system management.

Bused Interrupts

INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and NMIRQ* are bused signals between all STD 32 connectors, including Slot X. Bus Masters use these signals for interrupt signaling between peripherals or Bus Masters and other Bus Masters.

Slot-Specific Interrupts

Each of the first 15 slots of the STD 32 card cage has a dedicated interrupt between it and the Slot X connector (the last connector on the left side of the backplane). For Bus Masters that can interface to Slot X, this allows up to 15 interrupt sources in addition to the five bused interrupts.

Transfer CLASS	Nominal Transfer Rate	Burst Transfer Rate
SA8	2 Mbytes/second	N/A
SA16	4 Mbytes/second	N/A
EA8	4 Mbytes/second	N/A
EA16	8 Mbytes/second	16 Mbytes/second
EA32	16 Mbytes/second	32 Mbytes/second

Figure 5. *Theoretical bandwidths for STD 32 transfer types*

Multiprocessor Arbitration

The Slot X connector on STD 32 backplanes allows for a centralized arbitration scheme for up to 15 Bus Masters. Each slot has dedicated arbitration signals (MREQx*/MAKx*) which are used to gain control of the bus. EA Temporary Masters use the MREQx*/MAKx* signals for bus arbitration. SA Temporary Masters use a similar approach, but use the DREQx*/DAKx* signals for bus ownership. A centralized arbiter manages bus ownership between Temporary Masters and the Permanent Master. Rotating priority or optional fixed priority can be selected.

Compliance Levels

Compliance levels specify the capabilities of STD 32 board designs. Each bus-related feature, such as the ability to support EA or SA transfers, is given a mnemonic description to be used on data sheets and board specifications to assist customers in system configuration.

Board MODES

There are five board MODES within STD 32 as defined in **Figure 6**. MODES define how a board may be used. For instance, a CPU board would normally be a Permanent Master but when another Bus Master has control it might also support memory cycles to or from it by the Temporary Master. In this case the board would have two board MODES, Permanent Master and Memory Slave.

COMPONENT SIDE

Pin	Mnemonic	Signal Flow	Description
1	+5 VDC	In	Logic Ground
3	XA19	Out	Address
5	XA18	Out	Address
7	XA17	Out	Address
9	XA16	Out	Address
11	NOWS*	In	No Wait States
13	+5VDC	In	Logic Power
15	DAKx*	Out	DMA Acknowledge
17	GND	In	Logic Ground
19	D27	Bidir	Data
21	D26	Bidir	Data
23	D25	Bidir	Data
25	D24	Bidir	Data
27	D23	Bidir	Data
29	D22	Bidir	Data
31	D21	Bidir	Data
33	D20	Bidir	Data
35	GND	In	Logic Ground
37	D19	Bidir	Data
39	D18	Bidir	Data
41	D17	Bidir	Data
43	D16	Bidir	Data
45	GND	In	Logic Ground
47	IRQx	In	Interrupt Request
49	BE1*	Out	Byte Enable 1
51	BE0*	Out	Byte Enable 0
53	MEM16*	In	Memory 16-bit
55	M-IO	Out	Memory or I/O
57	DMAIOW*	Out	DMA I/O Write
59	IO16*	In	I/O 16-bit
61	CMD*	Out	Command
63	EX16*	In	Exchange 16-bit
65	EXRDY	In	Exchange Ready
67	INTRQ3*	In	Interrupt Request 3
69	MAKx*	Out	Master Acknowledge
71	SLBURST*	In	Slave Burst
73	XA27*	Out	Address
75	XA26*	Out	Address
77	XA25*	Out	Address
79	XA24*	Out	Address

CIRCUIT SIDE

Pin	Mnemonic	Signal Flow	Description
2	LOCK*	Out	Lock
4	XA23	Out	Address
6	XA22	Out	Address
8	XA21	Out	Address
10	XA20	Out	Address
12	RSVD	--	Reserved
14	+5VDC	In	Logic Power
16	DREQx*	In	DMA Request
18	GND	In	Logic Ground
20	D31	Bidir	Data
22	D30	Bidir	Data
24	D29	Bidir	Data
26	D28	Bidir	Data
28	GND	In	Logic Ground
30	D15	Bidir	Data
32	D14	Bidir	Data
34	D13	Bidir	Data
36	D12	Bidir	Data
38	D11	Bidir	Data
40	D10	Bidir	Data
42	D9	Bidir	Data
44	D8	Bidir	Data
46	MASTER16*	Out	Master 16-bit
48	AENx*	Out	Address Enable
50	BE3*	Out	Byte Enable 3
52	BE2*	Out	Byte Enable 2
54	GND	In	Logic Ground
56	W-R	Out	Write or Read
58	DMAIOR*	Out	DMA I/O Read
60	EX8*	In	Exchange 8-bit
62	START*	Out	Start
64	EX32*	In	Exchange 32-bit
66	T-C	Bidir	Terminate or Count
68	+5VDC*	In	Logic Power
70	MREQx	In	Master Request
72	MSBURST*	Out	Master Burst
74	XA31*	Out	Address
76	XA30*	Out	Address
78	XA29*	Out	Address
80	XA28*	Out	Address

Figure 4. *This table illustrates STD 32 Bus E Pinouts.*

STD 32 Board MODE	Definition
Permanent Master	Bus master that drives CLOCK*, monitors PBRESET*, and drives SYSRESET*
Temporary Master	Bus Master that requests the bus via BUSRQ*, MREQx, or DREQx*
I/O Slave	Slave that decodes and responds to SA or EA I/O cycles
Memory Slave	Slave that decodes and responds to SA or EA memory cycles
Arbiter (Mn,Dn)	System arbiter that manages n MREQx*/MAKx* signals and/or n DREQx*/DAKx* signals for arbitration

Figure 6. *STD 32 compliance board MODES*

Compliance CLASSES

For each board MODE, there are several CLASSES of transfers supported for that CLASS. Standard Architecture (SA) 8-bit and 16-bit transfer CLASSES are defined as SA8 and SA16 respectively. Extended Architecture (EA) 8-, 16-, and 32-bit transfer CLASSES are defined as EA8, EA16, and EA32, respectively.

Feature	Description	Additional Signal Support
A16	SA 16-bit I/O address decode (I/O Slave)/ generation (master)	A0-A15
A24	SA 24-bit memory address decode (Memory Slave)/generation (master)	A0-A24
D8	SA 8-bit data transfer, masters/slaves	D0-D7
D16	SA 16-bit transfer, masters/slaves	D0-D15,MEM16*,BHE*,IO16*
EBURST	EA Burst transfer capability, masters/slaves	SLBURST*,MSBURST*
EDMAA	EA type A DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx,DAKx*,T-C
EDMAB	EA type B DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx, DAKx*,T-C
EDMAC	EA type C DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx, DAKx*,T-C, SLBURST*, MSBURST*
GAX	EA geographical address support masters/slaves	AENx* (masters)
I	SA (STD-80) interrupt generation (slaves)/ servicing (masters) on INTRQ*, INTR1*,NMIRQ*, CNTRL* (INTRQ2*), or INTRQ3*	INTRQ*,INTRQ1*,NMIRQ* [CNTRL* (INTRQ2*)], INTRQ3*
ICA	Cascadable interrupt address support, masters/slaves	A8-A10 during INTA
IXP	Slot-specific interrupt servicing (Permanent Masters)/ generation (slaves), positive edge-triggered	IRQx
IXL	Slot-specific interrupt servicing (Permanent Masters)/ generation (slaves), low-level asserted	IRQx
MB	Bus arbitration via BUSRQ*/BUSAK* - SA Masters only	BUSRQ*,BUSAK*
MD	Bus Arbitration via DREQx*/DAKx* - SA Masters only	DREQx*, DAKx*
MX	Bus Arbitration via MREQx*/MAKx* (Permanent Master)/ request (Temporary Slave)	MREQx*,MAKx*
NOWS	No wait-state (NOWS*) support	NOWS*
SDMA8	8-bit SA frontplane DMA as specified in Chapter 2, masters/slaves	
SDMA16	16-bit SA frontplane DMA as specified in Chapter 2, masters/slaves	
XA16	EA 16-bit address decode, I/O transfers	A2-A15, BE0*-BE3* as per Chapter 3
XA32	Full 32-bit EA address space driven, masters may pull XA24*-XA31* passively high Full 32-bit EA address decoded by Memory Slaves	A2-A15, XA16-XA23, XA24* XA31*, BE0*-BE3*
XD8	8-bit EA data transfer, masters/slaves	D0-D7
XD16	16-bit EA data transfer, masters/slaves	D0-D15, EX16*, BE0*-BE3*
XD32	32-bit EA data transfer, masters/slaves	D0-D31, EX16*, EX32*, EX32* BE0* BE3*

Figure 7. *STD 32 compliance product descriptor feature listing*

Compliance Product Description

Features (Requirements/ Options)

Listed after the CLASS support for each board MODE is a string of required and/or optional features that the board supports. Requirements are items such as interrupt support or DMA that a board needs in order to operate. Options are items that may be used by a board but are not required for operation. Possible features for STD 32 compliance codes are found in **Figure 7**.

Compliance Style

Technical data sheets for STD 32-compatible boards include a product descriptor. This shows that the board complies with the STD 32 specification in all board MODES, transfer CLASSES, and required or optional features listed (see **Figure 8**).

For example, a board that can be either a Permanent Master or a Temporary Master with full EA8, EA16, EA32, SA8, and SA16 transfer CLASS support, interrupt support, cascade interrupt control, and that supports SA8 memory transfers to or from it when it is not in control, would have the following product descriptor:

STD 32 Compliance
Permanent Master: EA32, EA16, EA8, SA16, SA8 - MX, MB, ICA, I
Temporary Master: EA32, EA16, EA8, SA16, SA8 - {MX}, MB, ICA, I
Memory Slave: SA8

STD 32 Compliance
Permanent Master: Classes supported-{Requirements} Options
Temporary Master: Classes supported-{Requirements} Options
I/O Slave: Classes supported-{Requirements} Options
Memory Slave: Classes supported-{Requirements} Options
Arbiter (Mn, Dn): Classes supported-{Requirements} Options

Figure 8. *STD 32 compliance format*