STD BUS SPECIFICATION

16-Bit Data Transfers

I. INTRODUCTION

This document lists the changes and additions to the STD-80 rev 2.3 Bus Specification to support 16-bit data transfers for memory and I/O cards and expands memory addressing from 20- to 24-bits. These changes provide the foundation for more powerful 16 and 16/32-bit processor families such as the 680X0 and 80X86. The key design goal is downward compatibility with all existing STD Bus I/O mapped cards while supporting full 16-bit data transfers.

Assumptions

The following assumptions are made for 16-bit transfers:

* The card dimensions, bus connector, electrical requirements, and power supply voltage definitions remain the same as defined in the STD Bus Specification.
* CPU cards that support 16-bit transfers must be compatible with existing 8-bit I/O cards.
* New 16-bit memory cards may be required for CPU cards that support 16-bit transfers.
* MEMEX* is used (in conjunction with A0) to control 16-bit transfers.
* Interrupts are supported as in the STD Bus Recommended Practice.
* Supports CMOS and TTL STD Bus.

This specification allows new memory, I/O, and CPU cards to use a full 16-bit data path on the STD Bus, with data transferred as a low byte, high byte, or full word. New CPU cards must also switch between 8- and 16-bit data transfer modes in order to maintain compatibility with existing I/O cards, which always assume a low byte transfer.

II. FUNCTIONAL DESCRIPTION

16-Bit Bus Pinout

The Bus Connector Pin Assignment in Figure 1 shows the organization and pin-out. Signal flow direction is referenced to the current master. Descriptions of the signals that are redefined by this specification from the STD Bus 8088 rev 2.3 Specification are listed below.

16-Bit Signal Definitions

Data Bus (Pins 7-14, 16, 18, 20, 22, 24, 26, 28, 30). (16-bit, bidirectional, 3-state, active-high). Data Bus direction is controlled by the current master and is affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

All cards should release the data bus to a high-impedance state when not in use. The permanent master shall release the data bus in response to bus request (BUSRQ*) input from a temporary master, as in DMA transfers.

All data bus lines are multiplexed with 16 or the 24 bits of the address bus for address space expansion. The pin assignments for address expansion shall be as shown in Figure 2, the Bus Connector Pin Assignment table.

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power	2	+5VDC	In	Logic Power
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBATT	In	Battery Power	6	DCPWRDWN*	In	DC Power Down
DATA BUS	7	D3 (A19)	In/Out (Out)	Low-Order	8	D7 (A23)	In/Out (Out)	High Order
	9	D2 (A18)	In/Out (Out)	Low-Order	10	D6 (A22)	In/Out (Out)	High Order
	11	D1 (A17)	In/Out (Out)	Low-Order	12	D5 (A21)	In/Out (Out)	High Order
	13	D0 (A16)	In/Out (Out)	Low-Order	14	D4 (A20)	In/Out (Out)	High Order
ADDRESS BUS	15	A7	Out	Low-Order	16	A15 (D15)	Out(In/Out)	High Order
	17	A6	Out	Low-Order	18	A14 (D14)	Out(In/Out)	High Order
	19	A5	Out	Low-Order	20	A13 (D13)	Out(In/Out)	High Order
	21	A4	Out	Low-Order	22	A12 (D12)	Out(In/Out)	High Order
	23	A3	Out	Low-Order	24	A11 (D11)	Out(In/Out)	High Order
	25	A2	Out	Low-Order	26	A10 (D10)	Out(In/Out)	High Order
	27	A1	Out	Low-Order	28	A9 (D9)	Out(In/Out)	High Order
	29	A0	Out	Low-Order	30	A8 (D8)	Out(In/Out)	High Order
INTRQ1* CONTROL BUS	31	WR*	Out	Write Mem or I/O	32	RD*	Out	Read Mem or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Mem Address Select
	35	IOEXP	Out	I/O Expansion	36	MEMEX	Out	Memory Expansion
	37	INTRQ1*	In	Interrupt Req 1	38	MCSYNC*	Out	CPU Mach Cycle Sync
	39	STATUS1*	Out	CPU Status 1	40	STATUS0*	Out	CPU Status 0
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Int Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Int
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-button Reset
	49	CLOCK*	Out	Processor Clock	50	CNTRL*	In/Out	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUX GND	In	AUX Ground (bussed)
	55	AUX +V	In	AUX Positive (+12V DC)	56	AUX -V	In	AUX Negative (-12V DC)

* Low-level active indicator

NOTE: Address lines A16-A19 are multiplexed on data lines D0-D3 on each address cycle. Typically PCO and PCI are not
used on peripheral cards and should be connected together.

Bus Connector Pin Assignment

Address Bus (Pins 7-30). (24-bit, 3-state, active-high). The address originates at the current master. The permanent master shall release the address bus in response to a BUSRQ* input from a temporary master. The address bus provides 24-address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations.

PIN 36 MEMEX* - Byte high enable (3-state active-low). MEMEX* may originate from the current master and should be used to designate upper byte of full word transfers.

PIN 38 MCSYNC* - Machine Cycle Sync (3-state, active-low). This signal occurs once during each machine cycle of the processor. (Machine cycle is defined as the sequence that involves addressing, data transfer, and execution.) MCSYNC* keeps any peripheral device synchronized with the processor's operation. All STD Bus masters must provide MCSYNC* that meets the STD Bus Timing Specification.

This rising edge of this signal is used to latch the upper 8 address lines (A16-A23) on the low-to-high transition. On 16-bit memory and I/O cards, the rising edge is also used to latch address lines A8-A15.

16-Bit Data Transfers

The 16-bit data transfers are supported both for memory and I/O operations. Sixteen bit transfers consist of two simultaneous 8-bit transfers. A word is defined as two contiguous 8-bit bytes that begin on even address boundaries. Two signals on the STD Bus, A0 and MEMEX, uniquely specify the type of data transfer characteristic as either low byte, high byte or full word transfer. A0, the least significant bit of the Address Bus, specifies even or odd byte. MEMEX, the STD Bus memory expansion signal, defines upper byte or full word transfers. The truth table for data transfers to 16-bit cards is:

MEMEX	A0	CHARACTERISTIC
0	0	Whole word transfer (A8-15, D0-7)
0	1	Upper byte transfer (A8-15)
1	0	Lower byte transfer (D0-7)
1	1	None

The 80X86 family of processors generates the MEMEX and A0 signals directly through the use of the CPU control lines A0 and BHE* (byte high enable). The 68000 family uses the upper data strobe (UDS*) and lower data strobe (LDS*) to generate these control lines.

The MCSYNC* control signal is also generated by the 80X86 and 68000 family of processors as well. The relation of these control lines to the STD Bus is as follows:

STD BUS	80X86	68000
MCSYNC*	ALE	AS*
MEMEX	BHE*	UDS*
A0	A0	LDS*

Figure 2 diagrams both the 16-bit data transfer and 24-bit memory address relationships. The STD Bus Address and Data signals are divided into three groups: Low Address, Middle Address/High Data Bus, and Upper Address/Lower Data. The lower 8 address bits are latched and presented to the STD Bus on signal lines A0-A7. The upper 8 data bits, D8-D15 are multiplexed on the middle 8 address bits on the STD Bus A8-A15 signal lines. The upper eight bits of memory address (A16-A23) are multiplexed onto the data bus (D0-D7) respectively and are latched by memory cards on the rising edge (low-to-high transition) of MCSYNC*.

The relative timing for 16-bit data transfers is shown in Figure 2. Detailed timing is in Section 3.

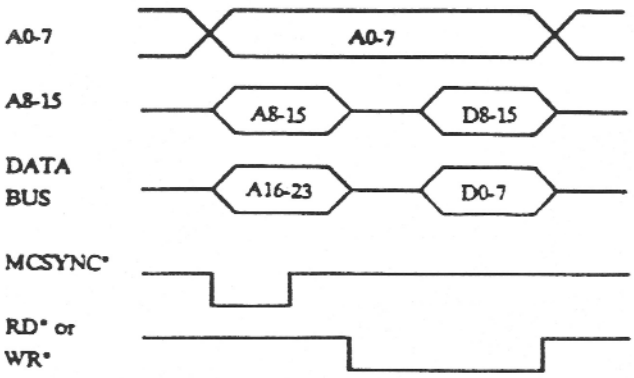


Figure 2. 16-Bit Data Multiplexing.

For full 16-bit data on the STD Bus, it simply requires multiplexing the high order data bits D8-D15 with the high order address bits A8-A15. Mapping is one-to-one so that D8-D15 is multiplexed on A8-A15, respectively. The combination of an active MEMEX (low) with the active edge of RD* or WR* shall latch the upper data byte. Timing requirements are the same as with the STD-80 rev. 2.3 specification so that D8-D15 shall be stable to meet the set-up and hold times required for proper transfers with respect to the Read (RD*) or Write (WR*) signals.

To remain compatible with existing 8-bit memory and I/O cards, buffer swap logic must be placed on 16-bit CPU cards to correctly route the data during I/O operations to 8-bit cards. When a high (odd) byte I/O read or write is issued to an 8-bit STD Bus I/O card, the CPU card must route the data to or from D0-D7 on the STD Bus vendor's and user's 8-bit I/O cards. Since MEMEX* is not decoded by most existing 8-bit I/O cards, then the MEMEX* signal becomes a don't care status during these data transfers to 8-bit cards.

24-Bit Memory Addressing

The 16-bit specification expands the memory range of the STD Bus from 20 to 24-bits to allow up to 16 megabytes of direct addressing. In the STD-80 rev. 2.3 Specification, 20-bit memory addressing is supported by multiplexing address and data at the beginning of each STD Bus cycle. The same decoding concept used in the 20-bit standard is valid for 24-bit memory addressing by defining four extra address lines, A20-A23, to be multiplexed on the data lines D4-D7 respectively.

III. ELECTRICAL SPECIFICATIONS

The Bus Write and Bus Read Timing from the STD-80 revision 2.3 specification is reproduced on the following pages with the addition of the address and data timing for 16-bit data transfers.

Data Transfer

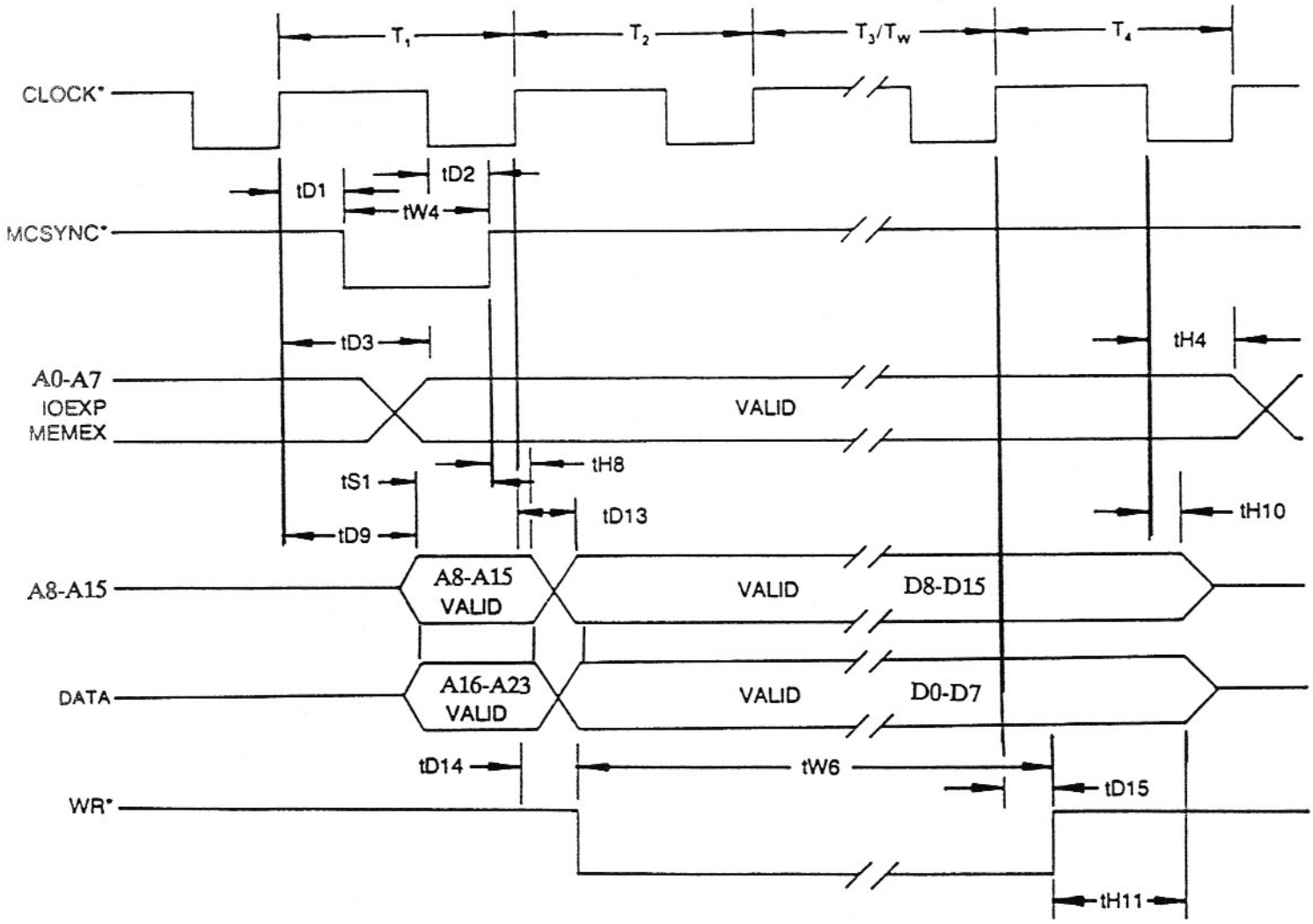
The Read and Write timing for 16-bit data transfers is shown in Figures 3 and 4. The timing is quite simple. It only requires specifications for set up and hold times to multiplex the data onto the bus. For full 16-bit data on the STD Bus, it simply requires multiplexing the high order data bits D8-D15 with the high order address bits A8-A15. The high order bits are latched into the card by RD* or WR*.

Addressing

Setup and hold timing for signals associated with the MCSYNC* and A16-A23 for latching the upper 8 address bits during 24-bit memory addressing are the same as defined in the STD-80 specification for latching A16-A23 for 20-bit addressing.

IV. MECHANICAL SPECIFICATIONS

No changes are required to the physical and mechanical specifications as detailed in Chapter 4 of the STD-80 rev 2.3 specification.

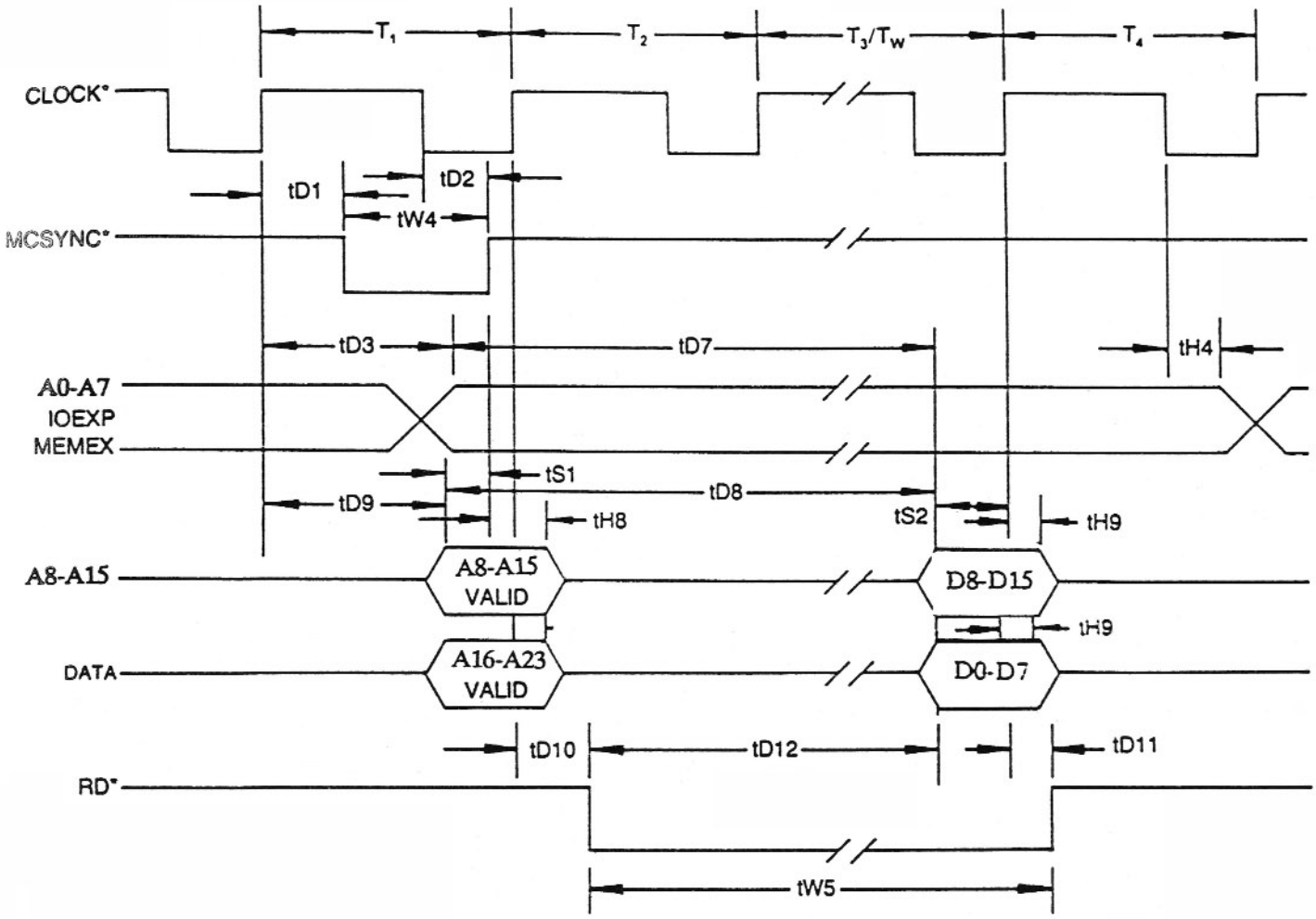


SYMBOL	PARAMETER	5.0 MHz		8.0 MHz	
		MIN.	MAX	MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low (1)	0	98	4	60
tD2	Delay from CLOCK* to MCSYNC* high	3	85	3	50
tD3	Delay from CLOCK* to Address 0- 7, MEMEX, IOEXP		130		75
tD9	Delay from CLOCK* to Address 8-23	0	125	0	73
tD13	Delay from CLOCK* to Data valid		122		97
tD14	Delay from CLOCK* to Advanced WR* low	0	92	8	86
tD15	Delay from CLOCK* to Advanced WR* high	0	90	8	71
tH4	Address 0- 7 MEMEX, IOEXP hold after CLOCK*	0		0	
tH8	Address 8-23 hold after MCSYNC*	20		10	
tH10	WR* Data hold after CLOCK*	0		0	
tH10	Data hold after Advanced WR* high	58		24	
tS1	Address 8-23 setup to MCSYNC*	15		15	
tW4	MCSYNC* pulse width	59		43	
tW6	Advanced WR* pulse width	335		210	

All times given in nanoseconds

(1) When the CPU inserts an I/O wait state, the MCSYNC* timing for 5MHz may be changed as follows: tD1 min. 0; max. 170. Although this allowance was not part of the original Bus Specification, it allows some manufacturers to generate MCSYNC* in a different manner. However, since it may not be compatible with some WAITRQ* implementations, caution is advised.

16-Bit Bus Write Timing.



SYMBOL	PARAMETER	5.0 MHz		8.0 MHz	
		MIN.	MAX	MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low (1)	0	98	4	60
tD2	Delay from CLOCK* to MCSYNC* high	3	85	3	50
tD3	Delay from CLOCK* to Address 0- 7		130		75
tD7	Delay from Address 0- 7 MEMEX, IOEXP to data valid	415		255	
tD8	Delay from Address 8-23 to data valid	415		255	
tD9	Delay from CLOCK* to Address 8-23	0	125	0	73
tD10	Delay from CLOCK* to RD* low	3	95	3	80
tD11	Delay from CLOCK* to RD* high	3	87	3	75
tD12	Delay from RD* to Data valid	260		140	
tH4	Address 0- 7 MEMEX, IOEXP hold after CLOCK*	0		0	
tH8	Address 8-23 hold after MCSYNC*	20		10	
tH9	RD* Data hold after CLOCK*	6		6	
tS1	Address 8-23 setup to MCSYNC*	15		15	
tS2	Data setup to CLOCK*	55		45	
tW4	MCSYNC* pulse width	59		43	
tW5	RD* pulse width	340		200	

All times given in nanoseconds

(1) When the CPU inserts an I/O wait state, the MCSYNC* timing for 5MHz may be changed as follows: tD1 min. 0; max. 170. Although this allowance was not part of the original Bus Specification, it allows some manufacturers to generate MCSYNC* in a different manner. However, since it may not be compatible with some WAITRQ* implementations, caution is advised.

16-Bit Bus Read Timing.

V. BUS PRACTICE

I/O Addressing - Because data is multiplexed on address lines A8-A15 during 16-bit-data I/O transfers, 16-bit-data I/O cards must latch A8-A15 on-card with MCSYNC* (as is done with memory addressing).

Most current 8-bit-data I/O cards decode at least 10 bits of I/O address (A0-A9) plus I/O expand (IOEXP), but do not latch any of the address lines. Since data is multiplexed on the upper address lines during 16-bit-data I/O transfers, some method must be used to prevent these cards from being incorrectly selected during a 16-bit I/O cycle, as these upper address lines will change when data is present during the I/O read or write cycle.

One method would be to use IOEXP as an enable for non-latching 8-bit-data I/O cards. IOEXP inactive (low) is currently used as an enable for I/O cards that decode only 8 address lines (A0-A7), and is driven low only for accesses to one block of 256 I/O ports (usually 0100-01FFh). I/O cards that decode a 10-bit I/O address and support IOEXP could also be mapped into this block of ports.

Another approach would be to leave possible conflicting I/O addresses vacant. For example, if a 16-bit-data I/O card were mapped at 01F0h, no current (non-latching) 8-bit-data card would be mapped at 0F0h, 2F0h, or 3F0h. Address lines A8 and A9 could then change during accesses to the 16-bit-data card without selecting an 8-bit-data card. In PC-compatible systems, port address ranges x50h-x5Fh and xE0h-xEFh can be used for 16-bit-data I/O ports without conflicting with any of the PC's reserved 8-bit-data ports.

It is recommended that 16-bit-data I/O cards decode the full 16-bit I/O address to make use of redundant addresses. It is also recommended that new 8-bit-data I/O cards latch A8-15, to avoid addressing problems in 16-bit systems.

8-bit Memory and I/O Compatibility: Compatibility with older 8-bit memory and I/O cards is possible with a number of different techniques. No specific technique is required by this specification.

One method allocates space in the memory and I/O maps which is defined for 8-bit data transfers only. For accesses to these areas, the master CPU is forced into 8-bit data transfers without regard for the instruction being executed. All data is routed to D0-D7 for transfers within this memory and I/O space, and word transfer operations are converted into two successive STD Bus byte operations for compatibility with existing 8-bit memory and I/O cards. Other memory and I/O areas are defined as 16-bit data, and have data routed over D0-D7 and/or D8-D15 as required.

Another technique, referred to as automatic bus sizing, lets the master CPU sample a status line driven by the memory or I/O card and decide whether that card will support 16-bit data transfers. If the response indicates an 8-bit boards, the CPU will automatically switch to 8-bit data transfers with all data routed to D0-D7. If the response indicates a 16-bit card, data is routed over D0-D7 and/or D8-D15 as required.

Automatic bus sizing is an option that can be implemented in both 16-bit CPU and I/O card designs. No STD Bus signals are allocated for use as 16-bit memory or 16-bit I/O status lines. If implemented, the practice for compatibility of these two 16-bit status lines is defined as:

Mechanical:

* Two connections for each 16-bit status line, with one being the status line and the other a ground.
* Connector pins are 0.025-in. square posts or equivalent
* This practice does not define the method for fastening the cable to the requesting card.
* Mating cables can be twisted pairs or flat cable.

Electrical:

* Low-level active signal
* LSTTL or high speed CMOS logic levels
* Drive sink capability of 20 mA at 0.4V
* Open collector/drain drive with 330 ohm pull-up resistor minimum.

16-bit Data Transfers - Word-wide data transfers to 16-bit memory and I/O card are handled in the same manner. MEMEX = 0 and A0 = 0 indicate a 16-bit data transfer on the STD Bus. All 16-bit data transfers must be on even word boundaries: A0 must always equal 0. The data is transferred in parallel on both the high and low data bytes of the STD Bus, D0 - D15.

8-bit Data Transfers to 16-bit Cards - Byte read and write operations are supported to 16-bit cards. MEMEX and A0 indicate whether the high or low byte of the 16-bits is being transferred. For both memory and I/O operations, an 8-bit low byte (A0 = 0 , MEMEX = 1) is transferred on the STD Bus low data bits D0 - D7, and an 8-bit high byte (A0 = 1, MEMEX = 1) is transferred on the STD Bus high data bits, D8 - D15.

Some 16-bit data cards designed prior to the release of this specification use D0 - D7 for 8-bit high byte data transfers. These cards can be used as 16-bit data cards in systems designed to this specification if 8-bit high byte data transfers are not used. Full 16-bit data transfers and low byte transfers are identical. Data transfers to 8-bit only I/O cards are <u>not</u> affected. CPU instructions that access these cards should be restricted to those that perform word or low byte access only. Manufacturers of these cards should note this in their literature.