SECTION 1
STD BUS Specifications

SCOPE
Application

The STD BUS defines an 8-bit microprocessor bus standard where the small card size in conjunction with LSI semiconductor technology creates a modular-by-function approach to control-oriented system design. The standard card size, connector and pinout lend itself to a bused motherboard that permits any card to work in any slot

The bus interface connector as shown in figure 1-1 is dedicated to microprocessor control of the card functions. Peripheral and I/O device connections are made at the edge of the card defined as the user interface. This concept gives an orderly signal flow across the card from the bus interface to the user interface. Peripheral and I/O devices can be connected to the system using their own unique connector and cabling requirements and complete functions can be modularly added to the system.
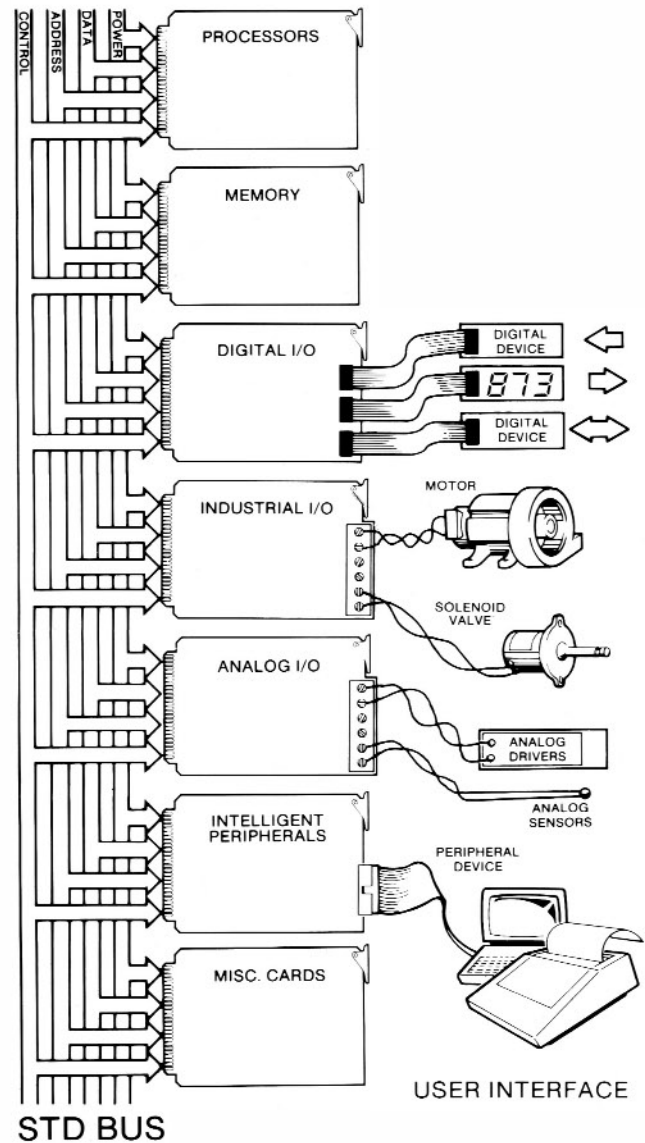

Figure 1-1. Bus Implementation

Inclusions

This document specifies:

- Card Dimensions
- Bus Connector
- Bus Pin Assignment
- Signal Definitions
- Electrical Requirements
- Read/Write Timing Sequences
- Read/Write Time Duration Parameters

Exclusions

This document does not specify:

- Card Functions
- User Interface
- Interchangeability

Definitions

- Shall: Shall signifies that which is mandatory
- Should: Should signifies that which is advisory

LOGICAL SPECIFICATIONS

Bus Pin Assignment. The BUS pinout is organized into five functional groups:

- Logic Power Bus: Pins 1-6
- Data Bus: Pins 7-14
- Address Bus: Pins 15-30
- Control Bus: Pins 31-52
- Auxiliary Power Bus: Pins 53-56

The organization and pinouts are shown in figure 1-2. Signal flow direction is referenced to the current master.

	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
		COMPONENT SIDE				CIRCUIT SIDE		
LOGIC POWER BUS	1	Vcc	In	Logic Power (+5 VDC)	2	Vcc	In	Logic Power (+5 VDC)
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBB #1/VBAT	In	Logic Bias #1/Bat Pwr	6	VBB #2/DCPD*	In	Logic Bias #2/Pwr Dwn
DATA BUS	7	D3/A19	In/Out	Data Bus/Address Ext	8	D7/A23	In/Out	Data Bus/Address Ext
	9	D2/A18	In/Out		10	D6/A22	In/Out	
	11	D1/A17	In/Out		12	D5/A21	In/Out	
	13	D0/A16	In/Out		14	D4/A20	In/Out	
ADDRESS BUS	15	A7	Out	Address Bus	16	A15	Out	Address Bus
	17	A6	Out		18	A14	Out	
	19	A5	Out		20	A13	Out	
	21	A4	Out		22	A12	Out	
	23	A3	Out		24	A11	Out	
	25	A2	Out		26	A10	Out	
	27	A1	Out		28	A9	Out	
	29	A0	Out		30	A8	Out	
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Pushbutton Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground	54	AUX GND	In	AUX Ground
	55	AUX +V	In	AUX Positive (+12 VDC)	56	AUX -V	In	AUX Negative (-12 VDC)

* Low-level active indicator

Figure 1-2. Bus Connector Pin Assignment

Signal Descriptions

Power Buses (Pins 1-6 and 53-56). The dual power buses accommodate logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns as shown in figure 1-3. Pins 5 and 6 provide for alternate use. If used for their alternate purpose these pins shall provide for disconnect capability on the card for conflict resolutions.

PIN	DESCRIPTION	COMMENT
1 & 2	Logic Power	Logic Power Source (+5 VDC)
3 & 4	Digital Ground	Logic Power Return Bus
5	Logic Bias Voltage	Low-current Logic Supply #1 (-5 VDC)
*5	Battery Backup Voltage	Alternate use as Battery Backup Voltage
6	Logic Bias Voltage	Low-current Logic Supply #2 (-5 VDC)
*6	DC Power Down	Alternate use as DC Power Down Signal
53 & 54	Auxiliary Ground	Auxiliary Power Return Bus
55	Auxiliary Positive	Positive DC Supply (+12 VDC)
56	Auxiliary Negative	Negative DC Supply (-12 VDC)

*PIN 5 VBAT—Battery Backup Voltage. VBAT is a DC voltage.
PIN 6—DCPD DC Power Down Signal. DCPD* is a logic signal that indicates Vcc has dropped below the recommended operating limit.

Figure 1-3. Power Bus Pin Assignments

Data Bus (Pins 7-14). (8-bit, bidirectional, 3-state, Active-High). Data Bus direction is controlled by the current master and is affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

All cards should release the data bus to a high-impedance state when not in use. The permanent master shall release the data bus in response to bus request (BUSRQ*) input from a temporary master, as in DMA transfers.

The Data Bus lines may be Multiplexed for address space expansion. The pin assignment for address expansion shall be as shown in figure 1-2.

Address Bus (Pins 15-30). (16-bit, 3-state, Active-High). The address originates at the current master. The permanent master shall release the address bus in response to a BUSRQ* input from a temporary master.

The address bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations. The particular microprocessor that is used determines the number of address lines and how they are applied.

The address bus may be extended by multiplexing on the data bus. The pin assignment for address expansion shall be as shown in figure 1-2.

PROCESSOR	NO. OF MEM ADDRESS LINES	ADDRESS LINES DURING REFRESH	No. of I/O Address Lines	
			I/O MAPPED I/O	MEMORY MAPPED I/O
8080	16	—	Lower 8	16
8085	16	—	Lower 8	16
Z80	16	Lower 7	Lower 8	16
6800	16	—	—	16
6809	16	—	—	16
6502	16	—	—	16
NSC800	16	Lower 8	Lower 8	16
8088	20	—	Lower 16	20

Figure 1-4. Examples of Address Bus Utilization

Control Bus (Pins 31-52). The control bus signal lines are grouped into five areas: memory and I/O control, peripheral timing, clock and reset, interrupt and bus control, and serial priority chain.

Memory and I/O Control lines provide the signals for fundamental memory and I/O operations. Simple applications may only require the following six control signals. All STD BUS cards shall support the memory and I/O control lines.

PIN 31 WR*—Write to memory or output (3-state, active-low). WR* originates from the current master and indicates that the BUS holds or will hold valid data to be written to the addressed memory or output device. WR* is the signal which writes data to memory or output ports.

PIN 32 RD*—Read from memory or input (3-state, active-low). RD* originates from the current master and indicates that it needs to read data from memory or from an input port. The selected input device or memory shall use this signal to gate data onto the BUS.

PIN 33 IORQ*—I/O request (3-state, active-low). IORQ* originates from the current master and indicates an I/O read or write or a special operation. It is used on the I/O cards and is gated with either RD* or WR* to designate I/O operations. For some processors, IORQ* is gated with other processor signals to indicate a special operation, IORQ* with STATUS 1* (M1*) indicates interrupt acknowledge for the Z80.

PIN 34 MEMRQ*—Memory request (3-state, active-low). MEMRQ* originates from the current master and indicates memory read or memory write operations or a special operation. It is used on memory cards and is gated with either RD* or WR* to designate memory operations. For some processors, MEMRQ* is gated with other processor signals to indicate a special operation, MEMRQ* with STATUS 1* (DT/R*) and STATUS 0* (SS0*) indicates Passive for the 8088.

PIN 35 IOEXP—I/O expansion (high expand, low enable). IOEXP may originate from any source and should be used to expand or enable I/O port addressing. An active-low shall enable primary I/O operations. I/O slaves shall decode IOEXP.

PIN 36 MEMEX—Memory expansion (high expand, low enable). MEMEX may originate from any source and should be used to expand or enable memory addressing. An active-low shall enable the primary system memory. MEMEX may be used to allow memory overlay such as in bootstrap operations. A control card may switch out the primary system memory to make use of an alternate memory. Memory slaves shall decode MEMEX.

Peripheral Timing Control Lines provide control signals that enable the use of the STD BUS with microprocessors that service their own peripheral devices. The STD BUS is intended to service any 8-bit microprocessor. Most peripheral devices work only with the microprocessor they are designed for. Four control lines of the bus are designated for peripheral timing. They are defined specifically for each type of microprocessor, so that it can best serve its own peripheral devices. In this way, the bus is not limited to only one processor.

PIN 37 REFRESH*—(3-state, active-low). REFRESH* may originate from the current master or from a separate control card and should be used to refresh dynamic memory. The nature and timing of the signal may be a function of the memory device or of the processor. In systems without refresh, this signal can be any specialized memory control signal. Systems with static memory may disregard REFRESH.*

PIN 38 MCSYNC*—Machine cycle sync (3-state, active-low). MCSYNC* shall originate from the current master. This signal should occur once during each machine cycle of the processor. MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal are processor-dependent. MCSYNC* keeps specialized peripheral devices synchronized with the processor's operation. It can also be used for controlling a bus analyzer, which can analyze bus operations cycle-by-cycle.

MCSYNC* should be used to de-multiplex extended addressing on the data bus.

PIN 39 STATUS 1*—Status control line 1 (3-state, active-low). STATUS 1* shall originate from the current master to provide secondary timing for peripheral devices. When available, STATUS 1* should be used as a signal for identifying instruction fetch.

PIN 40 STATUS 0*—Status control line 0 (3-state, active-low). STATUS 0* shall originate from the current master to provide additional timing for peripheral devices.

PROCESSOR	REFRESH* Pin 37	MCSYNC* Pin 38	STATUS 1* Pin 39	STATUS 0* Pin 40
8080	—	SYNC*	M1*	—
8085	—	ALE*	S1*	S0*
NSC800	REFRESH*	ALE*	S1*	S0*
8088	—	ALE*	DT/R*	SS0*
Z80	REFRESH*	(RD+WR+ INTAK)*	M1*	—
6800	—	φ1*	VMA*	R/W*
6809	—	EOUT* (φ2*)	—	R/W*
6809E	—	EOUT* (φ2*)	LIC*	R/W*
6502	—	φ2*	SYNC*	R/W*

*Low-level active
— Not used
R/W* Read high, write low
DT/R* Data transmit high, receive low

Figure 1-5. Peripheral Timing-Control Lines
for Various 8-Bit Microprocessors

Interrupt and bus control lines allow the implementation of such bus control schemes as direct memory access, multiprocessing, single stepping, slow memory, power-fail-restart, and a variety of interrupt methods. Priority for multiple interrupts or bus requests can be supported by either serial or parallel priority schemes.

PIN 41 BUSAK*—Bus acknowledge (active-low). BUSAK* originates from the permanent master and is used to indicate that the bus is available for use by a temporary master. The permanent master shall respond to a BUSRQ* by releasing the bus and giving an acknowledge signal on the BUSAK* line. BUSAK* should occur at the completion of the current machine cycle. The signal should be combined with a priority signal if multiple controllers need bus access.

PIN 42 BUSRQ*—Bus request (active-low, open collector/drain). BUSRQ* originates from a temporary master and causes the permanent master to suspend operations on the bus by releasing all 3-state bus lines. The bus should be released when the current machine cycle has been completed. BUSRQ* shall be used in applications requiring direct memory access (DMA). This signal can be an input, or an output, or it can be bidirectional, depending on the supporting hardware.

PIN 43 INTAK*—Interrupt acknowledge (active-low). INTAK* originates from the permanent master to indicate to the interrupting device that it is ready to respond to the interrupt. For vectored interrupts, the interrupting device shall place the vector address on the data bus during INTAK.* This signal can be combined with a priority signal, if multiple controllers need access to the permanent master. INTAK* is used in vectored interrupt schemes.

PIN 44 INTRQ*—Interrupt request (active-low, open–collector/drain. INTRQ* originates from any slave function to interrupt the processor on the permanent master. It should be masked and ignored by the processor, unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it should acknowledge by asserting INTAK* (pin 43). Other actions depend on the specific type of processor, the interrupt-related program instructions, and the hardware support of the interrupt mechanism.

PIN 45 WAITRQ*—Wait request (active-low, open-collector/drain). WAITRQ* may originate from any master or slave and shall cause the current master to suspend operations as long as it remains low. The current master should hold in a state that maintains a valid address on the address bus. WAITRQ* can be used to insert wait states in the processor cycle. Examples of its use include slow-memory operations and single stepping.

PIN 46 NMIRQ*—Nonmaskable interrupt (active-low, open–collector/drain). NMIRQ* may originate from any master or slave and shall be used as an interrupt input of the highest priority to the permanent master. It should be used for critical processor signaling, e.g., power-fail indications.

Clock and reset lines provide the bus with basic clock timing and reset capability.

PIN 47 SYSRESET*—System reset (active-low, open–collector/drain). SYSRESET* originates from any system reset circuit, which may be triggered by power-on detection, or by the pushbutton reset. All cards with circuits requiring initialization should decode SYSRESET.*

PIN 48 PBRESET* — Pushbutton reset (active-low, open–collector/drain). PBRESET* may originate from any card as an input to the system reset circuit.

PIN 49 CLOCK*—Clock from processor. CLOCK* originates from the permanent master and is a buffered, processor clock signal, for use in system synchronization or as a general clock source.

PIN 50 CNTRL*—Control. CNTRL* may originate from any card as an auxiliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real-time clock signal, or an external input to the processor.

Priority chain lines are provided for serial interrupt or bus control. Two bus pins are allocated to the chain, which requires logic on the card to implement the serial priority function. Cards not needing the chain shall jumper PCI to PCO on the card.

PIN 51 PCO-Priority chain out (active-high). PCO originates from every card as a signal sent to the PCI input of the next lower card in priority. A card that needs priority shall hold PCO low.

PIN 52 PCI—Priority chain in (active-high). PCI originates directly from the PCO of the next higher card in priority. A high level on PCI gives priority to the card sensing the PCI input.

Timing Specifications

Signal Time Sequence. The bus signal sequences are given for memory and I/O, read and write operations. The signal sequences are defined at the bus to guarantee card compatibility.

Address Selection Signal Sequences. The expansion signals, the address bus signals, and the request signals are used to select the data location for memory and I/O, read and write operations. These signals are referred to as the address selection signals.

- The expansion signal (MEMEX, IOEXP) is intended for selection of alternate memory or I/O address space.

- The address bus signals (A0-A23) are used to uniquely identify a data location within the memory or I/O space.

- The request signals (MEMRQ*, IORQ*) provide the selection between memory and I/O operations.

- The address selection signals may occur in any sequence. The last signal to become active and the first signal to become inactive determine the signal timing.

- The address selection signals shall all be stable prior to memory and I/O read and write operations.
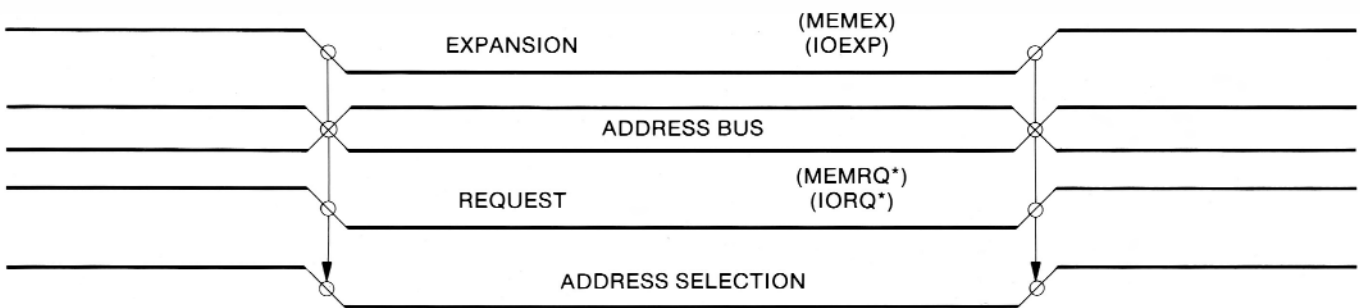

Figure 1-6. Address Selection Signal Sequence

Read Signal Sequences. The read sequence shown in figure 1-7 is controlled from the current master except for the data bus signals which are a response from the memory or I/O card.

The read signal causes a read operation to occur at the selected memory or I/O location. The read signal should change state within the address selection signal but may change at the same time. The trailing edge of the read signal shall indicate that the data has been transferred. The read signal shall hold the data bus active until the master accepts the data.

The data bus signals contain the data byte to be transferred to the master. These signals shall remain stable until the read signal is removed.
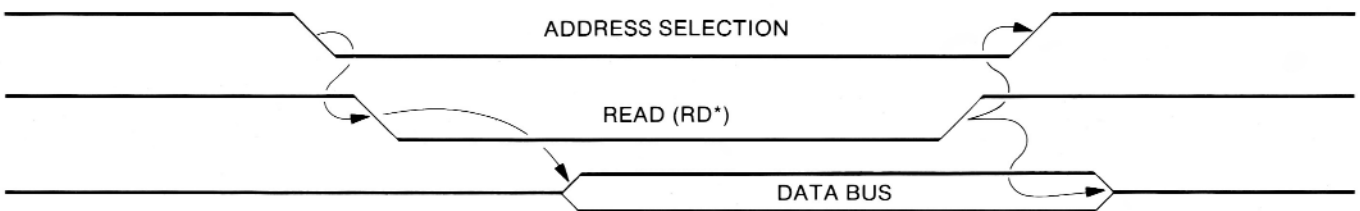

Figure 1-7. Read Signal Sequences

Write Signal Sequences. The write sequence shown in figure 1-8 is controlled from the current master. The address selection, data and write signals all originate from the current master.

The data bus signals contain the data byte to be transferred to memory or I/O. The data may occur before or after the leading edge of the write signal. The write signal shall change state within the address selection signal.
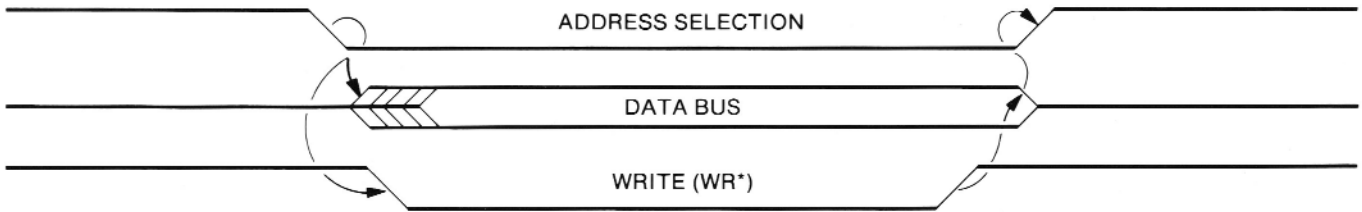

Figure 1-8. Preferred Write Signal Sequence

Signal Time Durations. Signal time durations are defined which will enable users to determine card compatibility for memory or I/O, read and write operations.

Read Timing. Critical read timing is shared between the current master and the memory or I/O card. The current master controls the read data access time (tARD) and has a requirement of a read data set-up time (tSRD). The memory or I/O device has a read access time (tAR) requirement. These timing relationships are shown in figure 1-9.
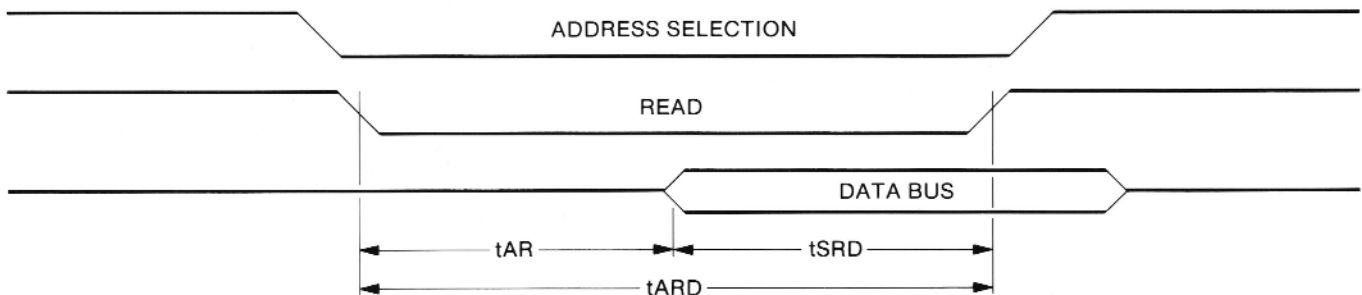

Figure 1-9. Critical Read Timing

Card compatibility for read operations shall be determined by comparing the specified required read access time of a memory or I/O card against the available read access time of a master card. Master card tAR shall be greater than or equal to Memory or I/O card tAR.

Master cards shall specify:

● tAR, maximum available Read Access time where tAR equals tARD minimum less tSRD minimum.

Memory or I/O cards shall specify:

● tAR, maximum required Read Access time. Since address selection may occur at the same time as Read, tAR must specify the worst case access time.

Write Timing. Critical write timing for compatibility is limited to the write data set-up time (tSWD) and write data hold time (tHWD) required by the memory or I/O card as shown in figure 1-10.

Card compatibility for write operations shall be determined by comparing the specified required write data set-up and hold times of a memory or I/O card against the available write data set-up and hold times of a master card.

- Master tSWD shall be greater than or equal to Memory or I/O tSWD.
- Master tHWD shall be greater than or equal to Memory or I/O tHWD.

Master cards shall specify:

- tSWD, minimum available write data set-up time.
- tHWD, minimum available write data hold time.

Memory or I/O cards shall specify:

- tSWD, minimum required write data set-up time.
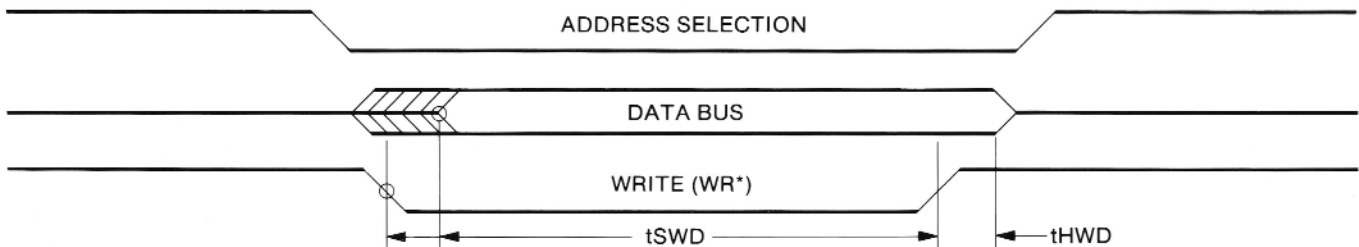- tHWD, minimum required write data hold time.

Figure 1-10. Critical Write Timing

Electrical Specifications

Maximum Ratings. The maximum ratings given in figure 1-11 for the bus card edge connector pins shall not be exceeded. These ratings are not recommended operating conditions as damage to card components is possible above these values.

Power Bus Voltage Tolerances. STD BUS cards require +5V for logic operations. Other operating voltages may be needed, according to individual card function and device types. The power signals measured at the card pins, not at the backplane traces, shall meet the voltage requirements given in figure 1-12.

PARAMETER	LIMIT	REFERENCE
Positive voltage applied to logic input or disabled 3-state output	+Vcc + 0.5 V	GND pins 3,4
Negative DC voltage applied to a TTL logic input or disabled 3-state output	-0.4V	
Negative DC voltage applied to a CMOS logic input or disabled 3-state output	-0.5V	

Figure 1-11. Maximum Voltage Ratings

CARD PIN	SIGNAL NAME	SUPPLY VOLTAGE	TOLERANCE	REFERENCE
1,2	TTL Vcc	+5V	±0.25V	GND pins 3,4
1,2	CMOS Vcc	+5V	±0.50V	GND pins 3,4
5	VBB #1	-5V	±0.25V	GND pins 3,4
5	VBAT	*	—	GND pins 3,4
6	VBB #2	-5V	±0.25V	GND pins 3,4
55	AUX +V	+12V	±0.5V	AUX GND pins 53, 54
55	AUX –V	-12V	±0.5V	AUX GND pins 53, 54

*VBAT may range from +3.5V to Vcc

Figure 1-12. Power Bus Voltage Ratings

Logic Signal Characteristics. The STD BUS is designed for compatibility with industry-standard TTL or high-speed CMOS logic levels. All logic signals shall meet the voltage requirements given in figure 1-13.

TTL BUS CARD PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OH} (high-state output voltage)	Vcc = MIN IOH=-3 mA	2.4	—	V
V_{OL} (low-state output voltage)	Vcc = MIN IOL=24 mA	—	0.5	V
V_{IH} (high-state input voltage)		2.0	—	V
V_{IL} (low-state input voltage)		—	0.8	V
CMOS BUS CARD PARAMETER	TEST CONDITIONS (–40° to 85°C)	MIN.	MAX.	UNITS
V_{OH} (high-state output voltage)	Vcc = MIN IOH=-6 mA	3.76	—	V
V_{OL} (low-state output voltage)	Vcc = MIN or MAX IOL=6 mA	—	0.37	V
V_{IH} (high-state input voltage)	Vcc = MIN[1]	3.15	—	V
	Vcc = MAX	3.85	—	V
V_{IL} (low-state input voltage)	Vcc = MIN	—	0.9	V

[1] The worst case V_{IH} occurs at Vcc = MAX.

Figure 1-13. Logic Signal Voltage Ratings

Bus Drive and Load Characteristics. Each card should present only one load per bus signal. Bus drivers should meet the IOL current sink requirements indicated in figure 1-13.

Mechanical Specifications

Card Dimensions. The circuit card shall meet the dimensions given in figures 1-14, 1-17, 1-18, 1-19 and 1-20. The dimensions exclude the card ejector and I/O interface connections.

Cards not meeting the minimum spacing of figure 1-14 shall specify actual spacing requirements.

CARD DIMENSIONS	INCHES		MILLIMETERS	
	NOMINAL	TOLERANCE	NOMINAL	TOLERANCE
Card Length	6.500	±0.025	165.10	±0.64
Card Height	4.500	+0.005,-0.025	114.30	+0.13,-0.64
Plated Board Thickness	0.062	+0.007,-0.003	1.58	+0.18,-0.08
Card Spacing	0.500	MIN	12.70	MIN

Figure 1-14. Card Dimensions

Card Profile Dimensions. Minimum card spacing requires a consideration for component height, lead protrusion, and card clearance, in addition to board thickness. Cards designed for minimum spacing shall meet the requirements of figure 1-15.

RECOMMENDED DIMENSIONS	INCHES		MILLIMETERS	
FOR MINIMUM CARD SPACING	MAXIMUM	MINIMUM	MAXIMUM	MINIMUM
Component Height	0.375	—	9.52	—
Component Lead Protrusion	0.040	—	1.02	—
Adjacent Card Clearance	—	0.010	—	0.25

Figure 1-15. Card Profile Dimensions for Minimum Spacing

Bus Connector. Bus connections shall be made via a printed circuit board card edge connector. The mating connector shall be a 56-pin (dual 28) card edge connector on 0.125 inch (3.18 mm) centers.

Card Ejector. Each card should use a single card ejector mounted on the top right corner as shown in figures 1-17 and 1-19.

Card Keying. Cards should be polarity keyed to prevent upside-down card insertion. Cards keyed for polarity shall have a single, offset keyslot located between pins 25 (26) and 27 (28) as shown in figure 1-16.

Cards keyed for position shall not use the slot between pins 27 (28) and 29(30), as this would invalidate the polarity keying.

0.050 ±0.005
(1.27 ±13 mm)

0.390
(9.9 mm)

KEY SLOT

25   (26)   EVEN
27   (28)   }   PINS ON
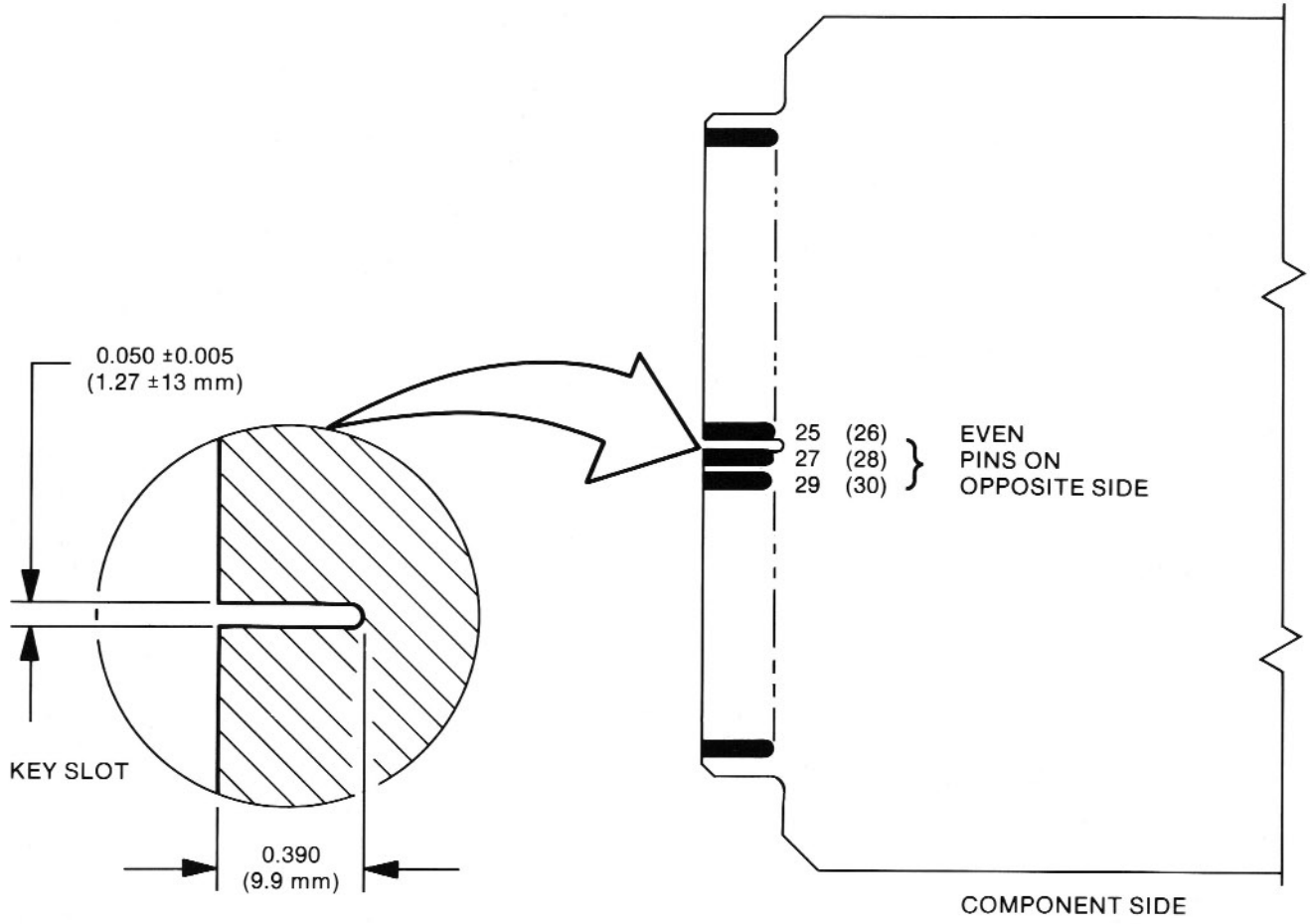29   (30)   OPPOSITE SIDE

COMPONENT SIDE

Figure 1-16. Key Slot Placement and Dimensions for Card Polarity Keying
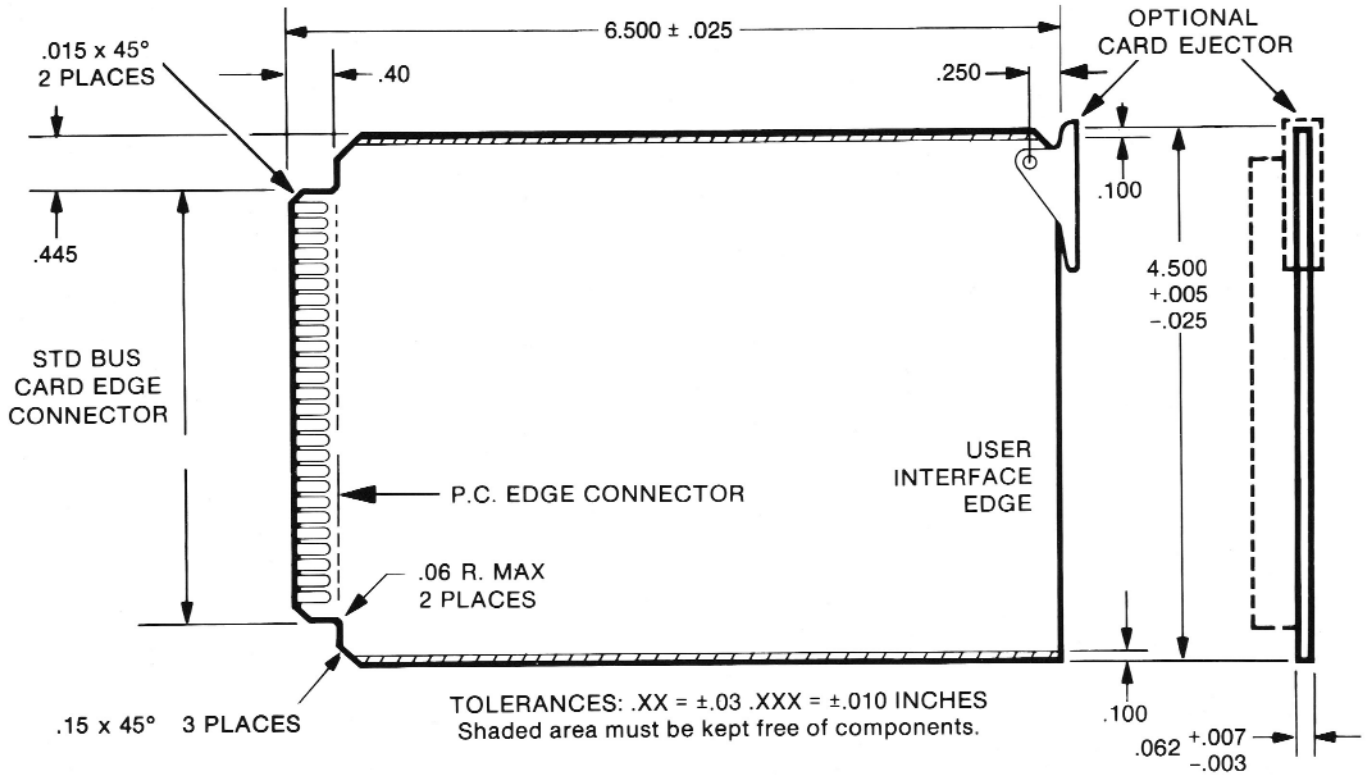
Figure 1-17. Bus Card Outline—Inches

Figure 1-18. Bus Edge Card Finger Design—Inches
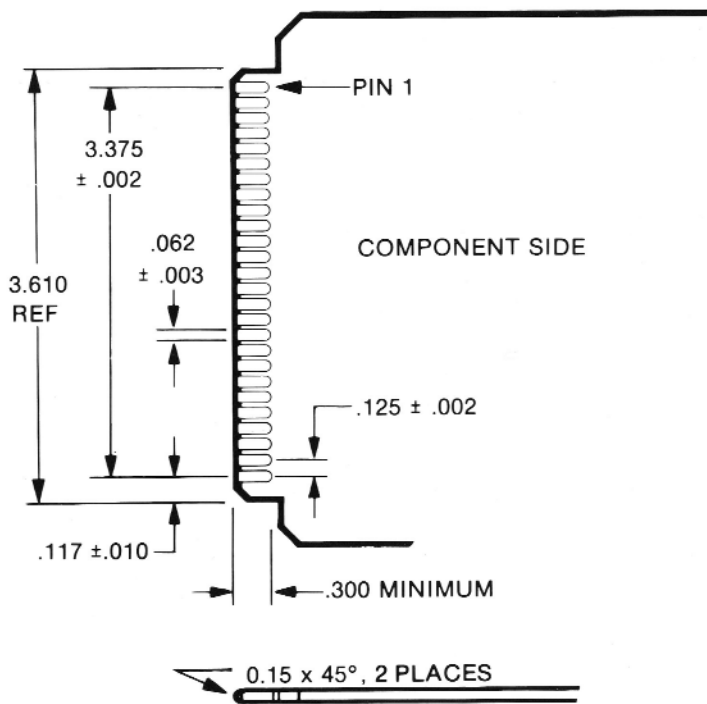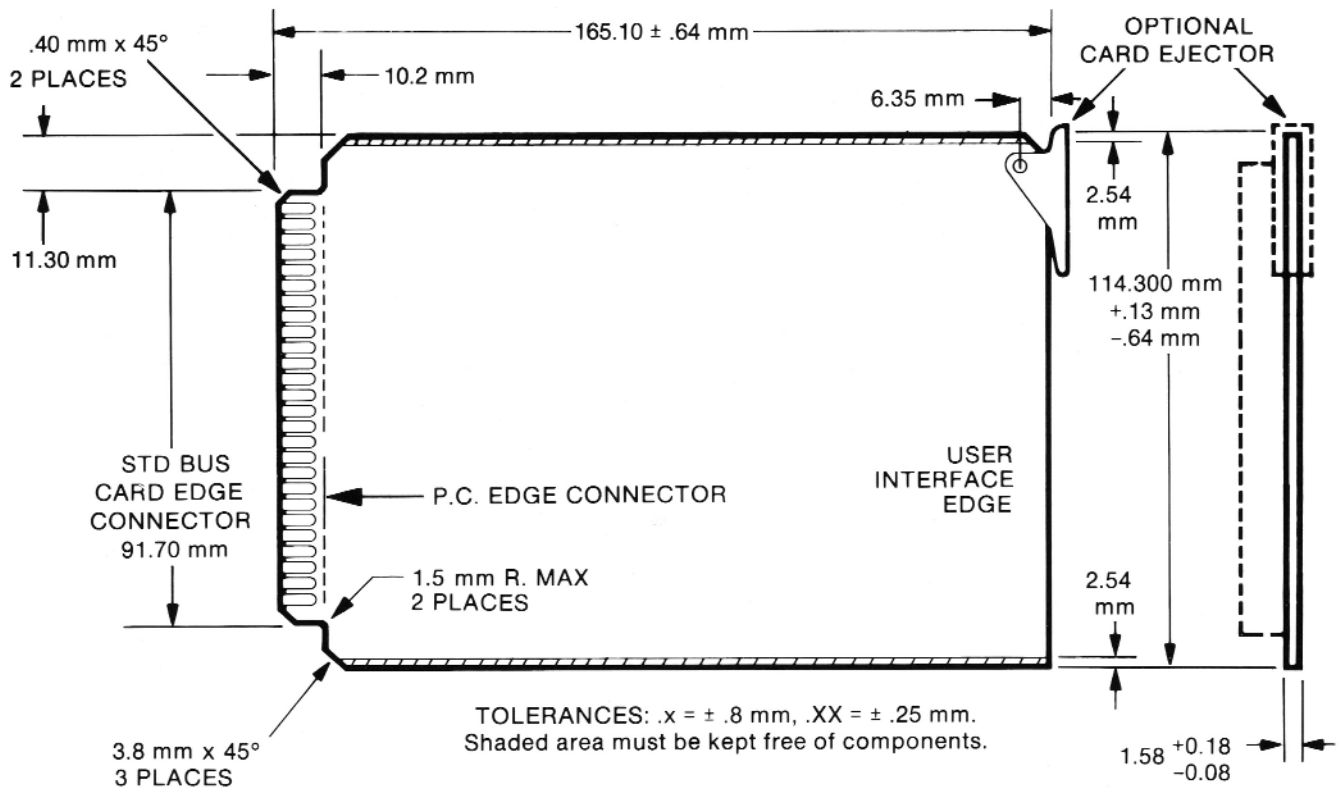
.40 mm x 45°
2 PLACES

10.2 mm

165.10 ± .64 mm

OPTIONAL CARD EJECTOR

6.35 mm

2.54 mm

11.30 mm

114.300 mm
+.13 mm
−.64 mm

STD BUS CARD EDGE CONNECTOR 91.70 mm

P.C. EDGE CONNECTOR

USER INTERFACE EDGE

1.5 mm R. MAX 2 PLACES

2.54 mm

3.8 mm x 45° 3 PLACES

TOLERANCES: .x = ± .8 mm, .XX = ± .25 mm.
Shaded area must be kept free of components.

1.58 +0.18 −0.08

Figure 1-19. Bus Card Outline—Metric

PIN 1

COMPONENT SIDE

91.70 mm REF

1.58 ± .08

85.70 ± .05 mm

3.18 ± .05 mm

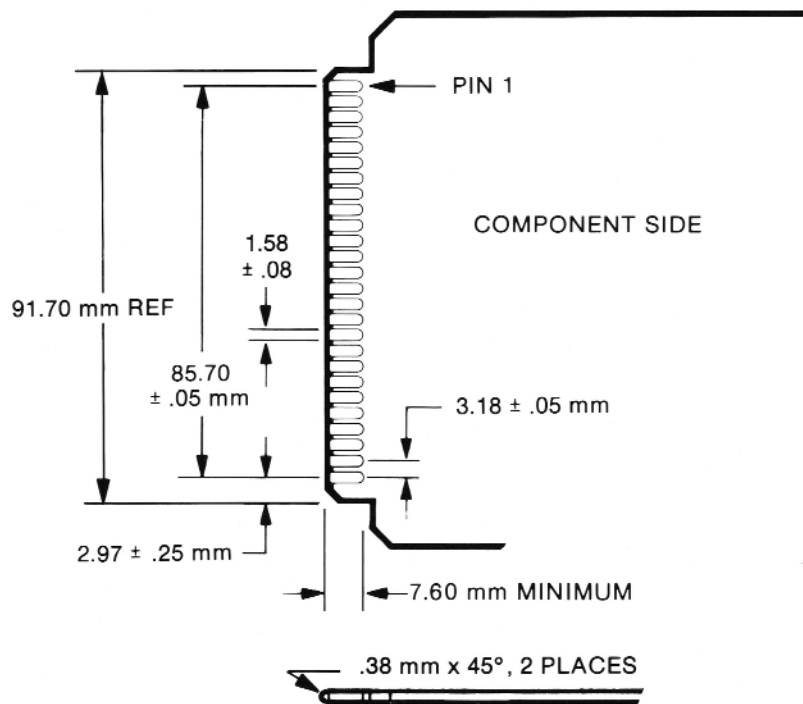**2.97 ± .25 mm**

7.60 mm MINIMUM

.38 mm x 45°, 2 PLACES

Figure 1-20. Bus Edge Card Finger Design—Metric