Reference Manual

STD-Z80 Bus Specification

VERSALOGIC
CORPORATION

STD-Z80 Bus Specification

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STDMG
STD MANUFACTURER'S GROUP

Table of Contents

STD Bus Pinout

The STD Bus pinout is organized into four functional groups:

- Dual Power Busses — Pins 1-6 and 53-56
- Data Bus — Pins 7-14
- Address Bus — Pins 15-30
- Control Bus — Pins 32-52

The organization and pinouts are shown in Table 1. This table lists the mnemonic function and signal flow direction (referenced to the processor card in control of the BUS) for each pin of the STD Bus. The STD Bus is further defined as requiring a 56-pin (dual 28) card edge connector, with 0.125-in. centers. Connectors are on a spacing interval of 0.5-in. centers minimum, and they accept the standard 4.5 x 6.5 x 0.062-in card.

COMPONENT SIDE				SOLDER SIDE			
Pin	**Signal**	**Flow**	**Description**	**Pin**	**Signal**	**Flow**	**Description**
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB#1/VBAT	In	Bias #1 / Battery backup	6	VBB#2 / PD*	In	Bias #2 / Power Down
7	D3	I/O	Data bus	8	D7	I/O	Data bus
9	D2	I/O	Data bus	10	D6	I/O	Data bus
11	D1	I/O	Data bus	12	D5	I/O	Data bus
13	D0	I/O	Data bus	14	D4	I/O	Data bus
15	A7	In	Address bus	16	A15	In	Address bus
17	A6	In	Address bus	18	A14	In	Address bus
19	A5	In	Address bus	20	A13	In	Address bus
21	A4	In	Address bus	22	A12	In	Address bus
23	A3	In	Address bus	24	A11	In	Address bus
25	A2	In	Address bus	26	A10	In	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	A0	In	Address bus	30	A8	In	Address bus
31	WR*	In/Out	Write strobe	32	RD*	In/Out	Read strobe
33	IORQ*	In/Out	I/O addr. select	34	MEMRQ*	In/Out	Memory addr. select
35	IOEXP	Out	I/O expansion	36	MEMEX	In/Out	Memory expansion
37	REFRESH*	Out	Refresh timing	38	MCSYNC*	Out	Machine cycle sync.
39	STATUS1*	Out	CPU status	40	STATUS0*	Out	CPU status
41	BUSAK*	Out	Bus acknowledge	42	BUSRQ*	In	Bus request
43	INTAK*	Out	Interrupt acknowledge	44	INTRQ*	In	Interrupt request
45	WAITRQ*	In	Wait request	46	NMIRQ*	In	Non-maskable interrupt
47	SYSRESET*	Out	System reset	48	PBRESET*	In	Push button reset
49	CLOCK*	Out	CPU clock	50	CNTRL*	In	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	In	±12 volt ground	54	AUXGND	In	±12 volt ground
55	AUX+V	In	+12 volt input	56	AUX-V	In	–12 volt input

* Denotes an active low signal.

Table 1. STD Bus Pinout

STD-Z80 Signal Definitions

Dual Power Busses (Pins 1-6 and 53-56)

The dual power busses accommodate logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns as shown.

Pin	Description	Comments
1 & 2	Logic Power	Logic Power Source (+5Vdc)
3 & 4	Digital Ground	Logic Power Return Bus
5	Logic Bias Voltage	Low-current Logic Supply #1 (-5Vdc) or Battery Backup Voltage
6	Logic Bias Voltage	Low-current Logic Supply #2 (-5Vdc) or DC Power Down Signal
53 & 54	Auxiliary Ground	Auxiliary Power Return Bus
55	Auxiliary Positive	DC Supply (+12Vdc)
56	Auxiliary Negative	DC Supply (-12Vdc)

Table 2. Power Busses

Data Bus (Pins 7-14)

The data bus is an 8-bit, bidirectional, 3-state bus. (Bidirectional means signals may flow either into or out of any card on the bus.) Direction of data is normally controlled by the processor card via the control bus. The data direction is normally affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

The data bus uses high-level active logic. All cards are required to release the bus to a high-impedance state when not in use. The processor card releases the data bus in response to bus request (BUSRQ*) input from an alternate system controller, as in DMA transfers.

Z80 peripheral devices monitor the opcode stream for an RETI instruction for automatic interrupt dismissal. The STD-Z80 data bus must always contain opcodes being executed by the CPU.

Address Bus (Pins 15-30)

The address bus is a 16-bit, 3-state, high-level active bus. Normally, the address originates at the processor card. The card releases the address bus in response to a BUSRQ* input from an alternate controller.

The address bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations.

The 16-bit Z80 address is applied directly to the 16 STD BUS address lines. The address bus provides a 16-bit memory address, an 8-bit I/O address or a 7-bit refresh address.

I/O addressing uses the lower 8 address bits of the 16-bit address bus, and occurs during I/O instruction execution. Refresh addressing for dynamic RAMs uses the lower 7 address bus lines. The refresh address occurs during the T_3 and T_4 time states of an M1 machine cycle.

Control Bus (Pins 31-52)

The control bus determines the flexibility of the STD Bus. Signal lines are grouped into five separate areas: memory and I/O control, peripheral timing, clock and reset, interrupt and bus control, and serial priority chain.

Memory and I/O Control

Memory and I/O Control lines provide the signals for fundamental memory and I/O operations. Simple applications may only require the following six control signals:

WR* Write to memory or I/O (3-state, active-low), pin 31. Z80 WR*

This signal indicates that the bus holds valid data to be written in the addressed memory or output device. WR* is the clock pulse, which writes data to memory or output port latches. The signal originates from the processor, which also provides the output data on the bus.

RD* Read from memory or I/O (3-state, active-low), pin 32. Z80 RD*

This signal indicates that the processor or other bus-controlling device needs to read data from memory or from an I/O device. The selected I/O device or memory utilizes this signal to gate data onto the data bus. RD* originates from the processor, which accepts the data from the data bus.

IORQ* Input / Output request (3-state, active-low), pin 33. Z80 IORQ*

This signal indicates that the address lines hold a valid I/O address for an I/O read or write. It is used on the I/O cards and is gated with either RD* or WR* to designate I/O operations. If STATUS1* is also asserted, the IORQ* signal indicates that an interrupt acknowledge is in progress.

MEMRQ* Memory request (3-state, active-low), pin 34. Z80 MEMRQ*

This signal indicates that the address bus holds a valid address for memory read or write operations. It is used on memory cards and is gated with either RD*, REFRESH*, or WR* to designate memory operations.

IOEXP I/O expansion (high expand), pin 35.

This signal expands or enables I/O port addressing. An active-low enables primary I/O operations. An example of its use is to allow common address decoding in memory-mapped I/O operations. Simple systems can generally strap this signal to ground.

MEMEX Memory expansion (high expand), pin 36.

This signal expands or enables memory addressing. An active-low enables the primary system memory. MEMEX allows memory overlay such as that found in bootstrap operations. It has the same general timing as an address line. MEMEX may be decoded by all memory cards as an expansion signal but will be ignored by memory boards that reside in both memory spaces. A control card may switch out the primary system memory to make use of an alternate memory. Simple systems can generally strap this signal to ground.

Peripheral Timing Control

Peripheral timing control lines provide control signals that enable the use of the STD Bus with microprocessors that service their own peripheral devices. The STD Bus is intended to service any 8-bit microprocessor. Most peripheral devices work only with the microprocessor they are designed for. Four control lines of the STD Bus are designated for peripheral timing. They are defined specifically for each type of microprocessor, so that it can best serve its own peripheral devices. In this way, the STD Bus is not limited to only one processor.

REFRESH* Dynamic Memory Refresh (3-state, active-low), pin 37. Z80 RFSH*

This signal refreshes dynamic memory. It may be generated on the processor card or on a separate control card. Simple systems with static memory may disregard REFRESH*.

The Z80 microprocessor chip is specifically designed for refreshing some standard dynamic RAM chips. These devices can be refreshed transparently during the opcode fetch memory cycle without complex processor synchronization circuitry and without delaying processor instruction execution time.

The REFRESH* output signal occurs during T_3 and T_4 of the opcode fetch cycle, and is used to indicate that a memory refresh address is present on the address bus. The address is composed of a presettable, auto-counting 7-bit address (A0-A6) which is the lower seven bits of the Z80's R register., an eighth bit (A7) which is the R register's most significant bit and is program-settable in the high or low state.

The RD* signal will not be active during the refresh cycle to prevent data from different memory locations from being gated onto the data bus. During refresh time, the MEMRQ* signal should be used to perform the refresh of memory elements as the address bus is stable only during MEMRQ* time.

MCSYNC* Machine cycle sync (3-state, active-low), pin 38. For the Z80, MCSYNC* = RD + WR + (IORQ*)(M1*)

This signal occurs once during each machine cycle of the processor. (Machine cycle is defined as the sequence that involves addressing, data transfer, and execution.) MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal are processor dependent. MCSYNC* keeps specialized peripheral devices synchronized with the processor's operation. It can also be used for controlling a bus analyzer, which can analyze bus operations cycle-by-cycle.

MCSYNC* is obtained by ORing the read, write and interrupt acknowledge signals. Thus MCSYNC* occurs once in each machine cycle and can be used to allow a logic signal analyzer to select a specific cycle within a multi-cycle instruction for analysis. The timing of MCSYNC* varies according to machine cycle type.

STATUS 1* Status control line 1 (3-state, active-low), pin 39. Z80 M1*

This signal provides secondary timing for peripheral devices. When available, STATUS 1* is considered as a signal for identifying instruction fetch.

STATUS 1* is equivalent to the Z80's M1* signal, which denotes the opcode fetch or interrupt acknowledge cycle (M1* is ANDed with IORQ* internally to produce INTAK, and externally with MEMRQ* to denote opcode fetch). Note that the Z80 has both 1-byte and 2-byte opcodes (2-byte opcodes are identified by a first byte equal to CB, DD, ED, or FD hexadecimal). Accordingly, the processor asserts STATUS 1* in each opcode byte, or twice per instruction cycle for these instructions.

STATUS 1* will also be asserted early in the interrupt acknowledge cycle, before INTAK* is asserted. The peripheral devices should freeze their ability to change the PCO line when STATUS 1* is asserted to allow the ripple priority daisy chain to propagate through the peripheral devices. When STATUS 1* is asserted, an interrupting peripheral may continue to assert its PCO line low. If a peripheral is not interrupting, PCO should be the same as PCI.

STATUS 0* Status control line 0 (3-state, active-low), pin 40.

This signal has no standard use for STD Z80 systems.

Interrupt and Bus Control

Interrupt and bus control lines allow the implementation of such bus control schemes as direct memory access, multiprocessing, single stepping, slow memory, power-fail-restart, and a variety of interrupt methods. The STD Bus includes provision for a serial priority chain. Parallel priority schemes can also be implemented.

BUSAK* Bus acknowledge (active-low), pin 41. Z80 BUSAK*

This signal indicates that the bus is available for use by a requesting controller. The controlling processor responds to a BUSRQ* by releasing the bus and giving an acknowledge signal on the BUSAK* line. BUSAK* occurs at the completion of the current machine cycle.

BUSRQ* Bus request (active-low, open collector), pin 42. Z80 BUSRQ*

This signal causes the controlling processor to suspend operations on the STD Bus by releasing all 3-state STD Bus lines for use by another processor. The STD Bus is released when the current machine cycle has been completed. BUSRQ* is used in applications requiring direct memory access (DMA). In complex systems, it can be an input, or an output, or it can be bidirectional, depending on the supporting hardware.

INTAK* Interrupt acknowledge (active-low), pin43. Z80 (IORQ*)(M1*)

This signal tells the interrupting device that the processor card is ready to respond to the interrupt. For vectored interrupts, the interrupting device places the vector address on the data bus during INTAK*. This signal can be used with the priority chain (PCI/PCO), if multiple controllers need bus access. INTAK* does not occur as a response to an NMIRQ*. The INTAK* cycle includes two wait states to allow sufficient time for the priority chain signals to stabilize and identify which I/O device must insert the response vector. Additional wait states may be added to the interrupt acknowledge cycle. The processor allows three software controlled uses of INTAK* (IM0, IM1, IM2). In interrupt mode 0 (IM0), the processor accepts the data on the data bus as an opcode to be executed. In M1, the processor ignores the vector, and an internal vector will be generated. In IM2, the processor accepts the data bus as a vector to an address where the address of the interrupt service routine will be found. In IM2, the least significant bit of the vector from the peripheral must be 0. INTAK* corresponds to a logical AND of STATUS 1* and IORQ*

INTRQ* Interrupt request (active-low, open collector), pin 44. Z80 INT*

This processor-card input signal conditionally interrupts the program. It is masked and ignored by the processor, unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it usually acknowledges by asserting INTAK* (pin 43).

WAITRQ* Wait request (active-low, open collector), pin 45. Z80 WAIT*

This input signal to the processor suspends operations as long as it remains low. Normally, the processor holds in a state that maintains a valid address on the address bus. WAITRQ* can be used to insert wait states in most machine cycles. Examples of its use include slow-memory operations and single stepping. Any device which needs a wait state should assert WAITRQ* on the bus to signal the bus master to wait.

NMIRQ* Nonmaskable interrupt (active-low, open collector), pin 46. Z80 NMI*

This signal is a processor-card interrupt input of the highest priority. It should be used for critical processor signaling, e.g., power-fail indications. The NMIRQ* line is edge activated.

Clock and Reset

Clock and reset lines provide the STD Bus with basic clock timing and reset capability.

SYSRESET* System reset (active-low), pin 47.

This signal is an output from the system reset circuit, which is triggered by power-on detection, or by the push-button reset. The system reset bus line should be applied to all bus cards that have latch circuits requiring initialization. The SYSRESET* signal may be an input, an output or bidirectional, depending on the supporting hardware.

PBRESET* Push-button reset (active-low), pin 48.

This signal is an input line to the system reset circuit.

CLOCK* Clock from processor, pin 49.

This signal is a buffered, processor clock signal, for use in system synchronization or as a general clock source.

CNTRL* Control, pin 50.

This signal is an auxiliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real-time clock signal, or an external input to the processor.

Serial Priority Chain

Serial priority chain lines are provided for interrupt or data bus control Two bus pins are allocated to the chain, which requires logic on the card to implement the priority function. Cards not needing the chain must jumper PCI to PCO on the card, if they are to be used in a serial priority scheme.

PCO Priority chain out (output, non-bussed), pin 51.

This signal is sent to the PCI input of the next lower card in priority. A card requesting an interrupt should hold PCO low. If a card is not interrupting, PCO should follow PCI.

The peripheral card shall freeze its ability to change PCO if STATUS 1* is asserted. The only PCO changes possible when STATUS 1* is asserted shall be due to the PCI input changing. This allows time for the priority chain to propagate.

In a vectored interrupt system, an interrupting device that is not yet acknowledged shall also drive it's PCO line high if the first byte of a two byte opcode fetch is an ED, and the second byte is being fetched.

This allows a lower priority interrupted and acknowledged device to sense the return from interrupt condition. Each device shall sense the presence of the RETI instruction (ED 4D), and if the PCI input is high, shall clear its interrupting status. Once cleared, the device may then generate another interrupt.

PCI Priority chain in (input, non-bussed), pin 52.

This signal is provided directly from the PCO of the next higher card in priority. A high level on PCI gives priority to the card sensing the PCI input. An interrupting card may gate its vector onto the data bus when INTAK* is asserted and the PCI input is high. When a return from interrupt is sensed on the data bus, the interrupting device with priority will clear its interrupting status.

Electrical Specifications

Absolute Maximum Ratings

The maximum ratings for the STD Bus card edge connector pins, which are listed below, are not recommended operating conditions. Damage to card components is possible above these voltage levels. The specific voltage at which damage occurs is component-dependent.

Parameter	Limit	Reference
Positive DC voltage applied to logic input or disabled 3-state output	+5.5V	GND pins 3 & 4
Negative DC voltage applied to a logic input or disabled 3-state output	-0.4V	GND pins 3 & 4

Table 3. Absolute Maximum Ratings

Note: Unless otherwise specified, the removal of circuit cards that are compatible with the STD Bus, or the removal of their component parts from sockets, is not recommended while operating voltages are applied.

Power Bus Voltage Tolerances

STD Bus cards normally require +5V for logic operations. Other operating voltages may be needed, according to individual card function and device types. The table below shows the STD Bus power busses and voltage values. Note that these voltage values are specified at the card pins, not at the backplane traces.

Card Pin	Supply Voltage	Tolerance	Reference
1,2	Vcc (+5V)	±0.25V	GND pins 3 & 4
5	Vbb #1 (-5V)	±0.25V	GND pins 3 & 4
6	Vbb #2 (-5V)	±0.25V	GND pins 3 & 4
55	AUX +V (+12V)	±0.5V	AUX GND pins 53 & 54
56	AUX -V (-12V)	±0.5V	AUX GND pins 53 & 54

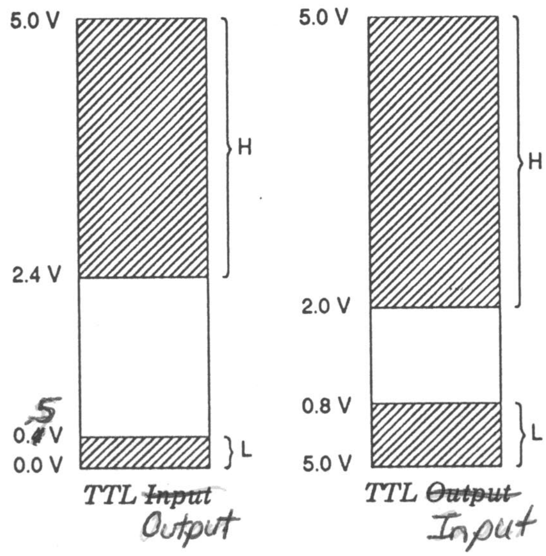
Table 4. Power Bus Voltage Tolerances

Logic Signal Characteristics

The STD Bus is designed for compatibility with industry-standard TTL logic. The following specifications apply over the specified temperature range for the STD Bus.

Std Bus Card Parameter		Test Conditions		Min	Max	Units
V_{OH}	(high-state output voltage)	V_{CC} = MIN	I_{OH} = 15mA	2.4	—	V
V_{OL}	(low-state output voltage)	V_{CC} = MIN	I_{OH} = 24mA	—	0.5	V
V_{IH}	(high-state input voltage)			2.0	—	V
V_{IL}	(low-state input voltage)			—	0.8	V
t_R, t_F	(rise time, fall time)			4	100	nS

Table 4. Logic Signal Characteristics



TTL Logic Levels

STD-Z80 Waveforms and Timing

Clock Requirements

The clock oscillator serves as the primary timing element in a Z80 based system. The oscillator's output drives the Z80 microprocessor, producing the time state clock. The time state clock's period is the shortest program-related period of time of interest in the system. Instruction execution times are computed as whole multiples of the time state clock period.

Crystal or External Clock Frequency	Resulting Time State Period	Comment
6 MHz	165 nS	Fastest allowable rate for Z80B device
4 MHz	250 nS	Fastest allowable rate for Z80A device
2.5 MHz	400 nS	Fastest allowable rate for Z80 device

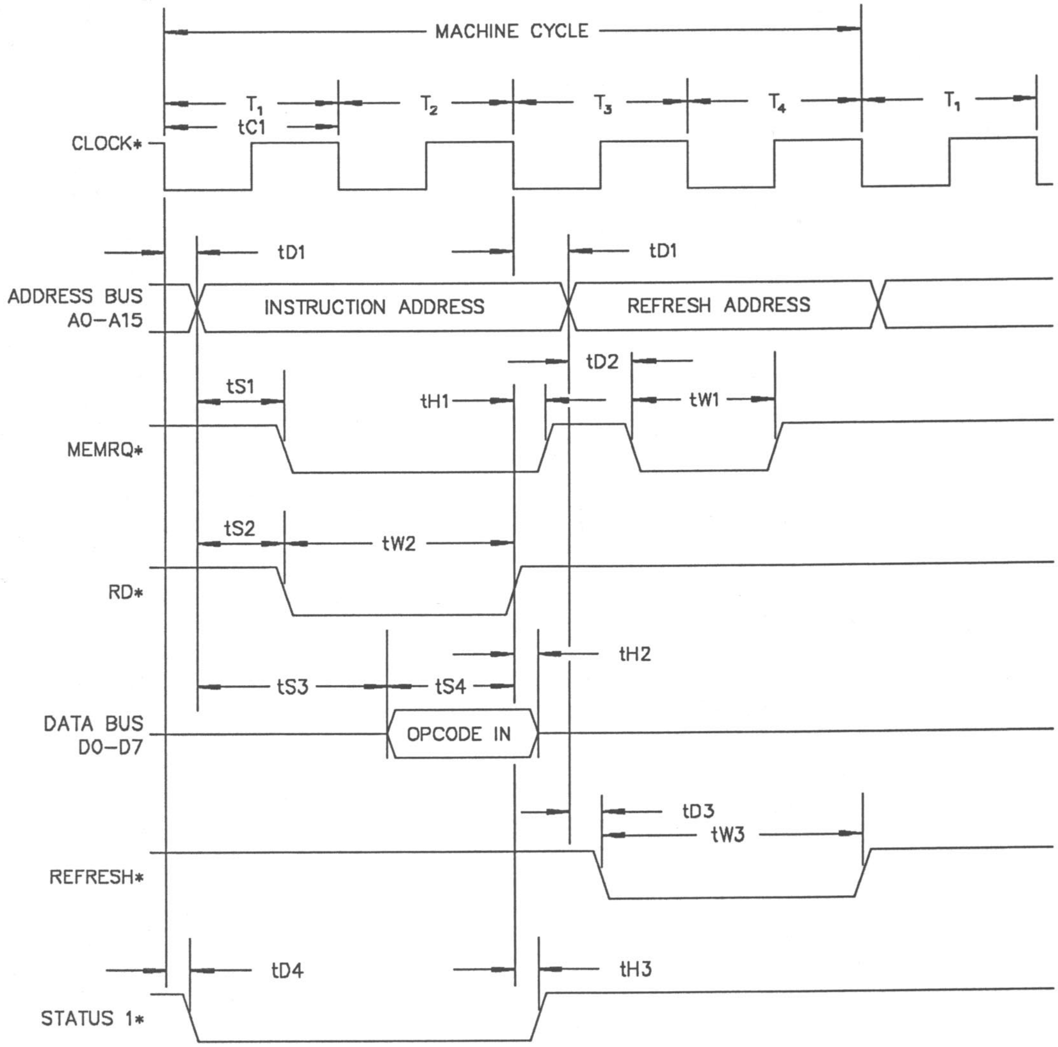
Table 6. Clock Oscillator Frequency Range

Timing Assumptions

These assumptions have been used during the preparation of the following timing diagrams.

1. All timing shown is for signals on the STD Bus and relative to the CLOCK* signal.
2. All signals from the processor card are buffered with a maximum propagation delay of 20 nS.
3. The timing values shown are representative of typical design practice. For critical applications it is the responsibility of the user to determine the applicability and suitability of these values.
4. All times are referenced to the mid point voltage given by $(V_L + V_H) / 2 = V_M$.
5. Clock rise time is maximum of 30 nS.

Opcode Fetch and Refresh Timing

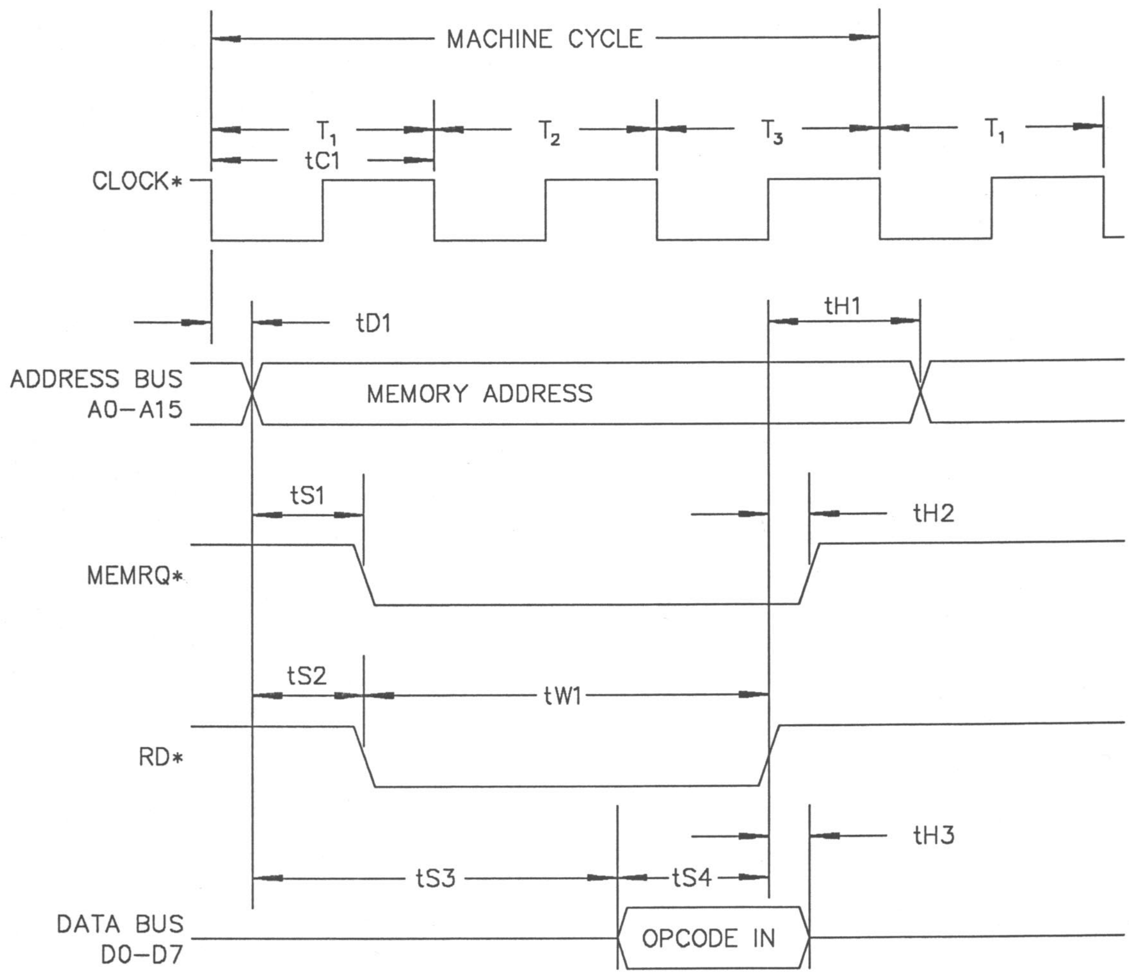


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tD2	MEMRQ* delay from Refresh Address valid		155		115		65
tD3	REFRESH* delay from Refresh Address valid		55		40		40
tD4	STATUS 1* delay from CLOCK*		150		120		100
tS1	Address setup before MEMRQ* active	90		30		15	
tS2	Address setup before RD* active	150		80		40	
tS3	Address setup before data valid	530		265		150	
tS4	Data setup before RD* inactive	155		125		105	
tH1	MEMRQ* hold time after RD* inactive	0		0		0	
tH2	Data hold time after RD* inactive	0		0		0	
tH3	STATUS 1* hold time after RD* inactive	15		0		0	
tW1	MEMRQ* pulse width (REFRESH)	335		195		115	
tW2	RD* pulse width	545		335		215	
tW3	REFRESH* pulse width	735		460		295	

Opcode Fetch and Refresh Timing

All times given in nanoseconds.

Memory Read Timing

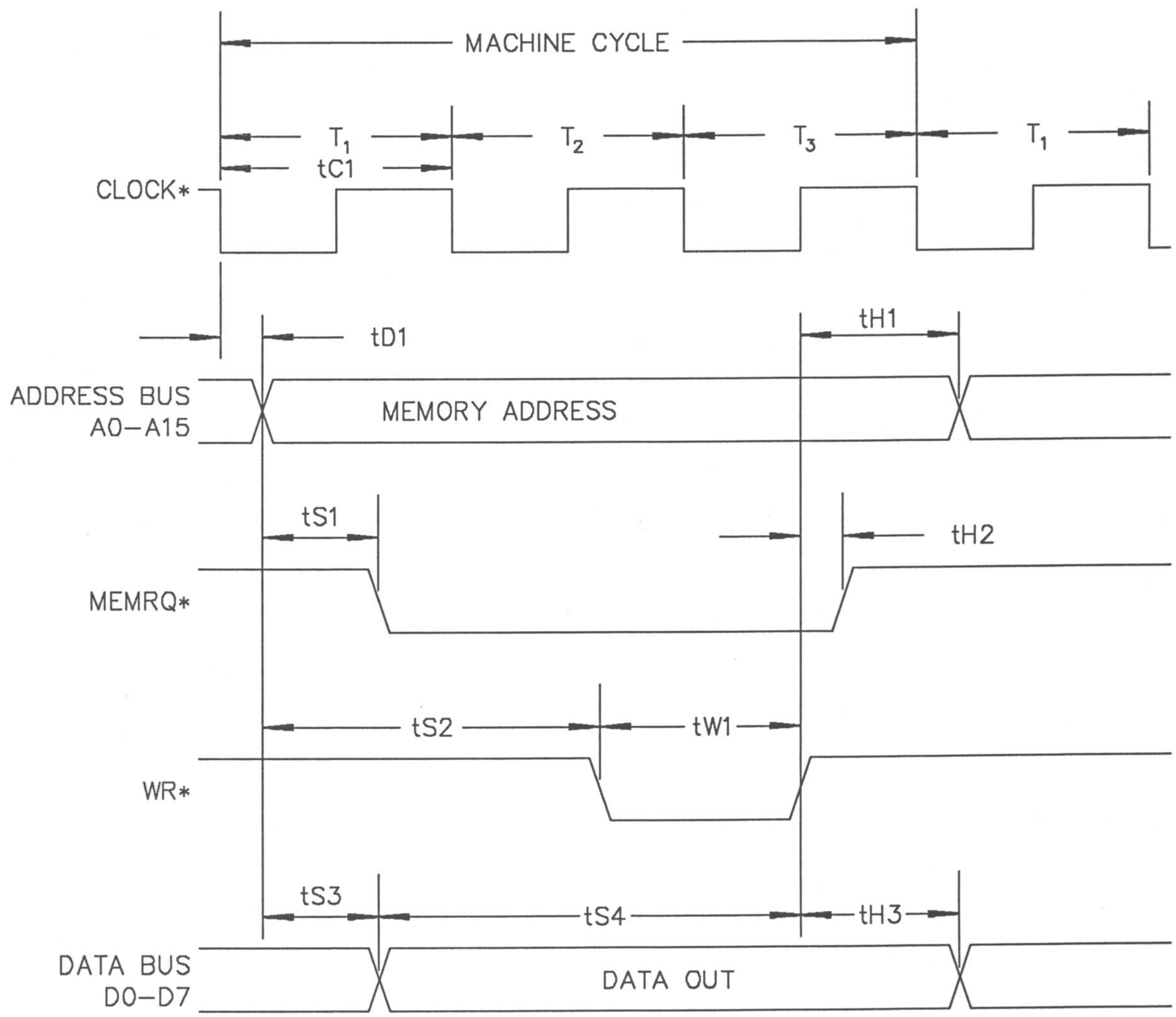


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tS1	Address setup before MEMRQ* active	90		30		15	
tS2	Address setup before RD* active	150		80		40	
tS3	Address setup before data valid	730		405		220	
tS4	Data setup before RD* inactive	165		140		115	
tH1	Address hold time after RD* inactive	125		45		15	
tH2	MEMRQ* hold time after RD* inactive	0		0		0	
tH3	Data hold time after RD* inactive	0		0		0	
tW1	RD* pulse width	760		465		295	

Memory Read Timing

All times given in nanoseconds.

Memory Write Timing

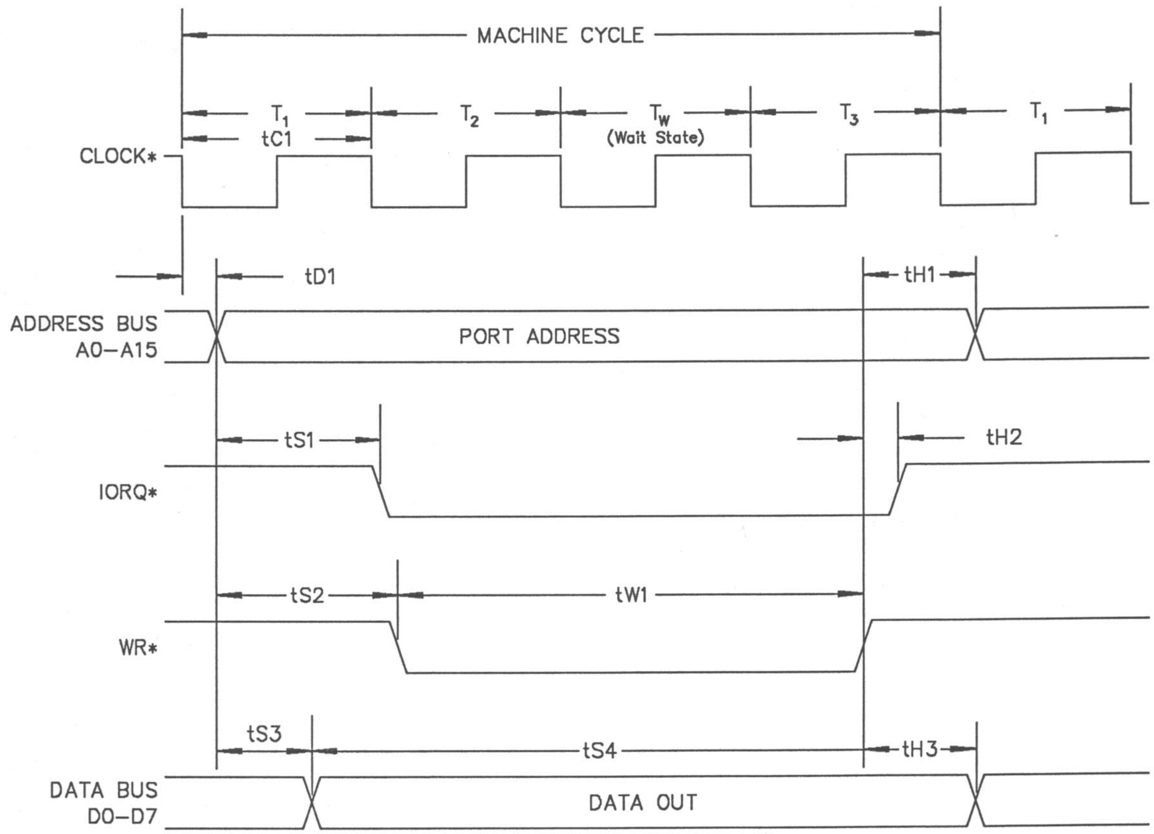


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tS1	Address setup before MEMRQ* active	90		30		15	
tS2	Address setup before WR* active	435		215		115	
tS3	Address setup before data valid	245		130		85	
tS4	Data setup before WR* inactive	530		280		145	
tH1	Address hold time after WR* inactive	125		45		15	
tH2	MEMRQ* hold time after WR* inactive	0		0		0	
tH3	Data hold time after WR* inactive	0		0		0	
tW1	WR* pulse width	335		195		115	

Memory Write Timing

All times given in nanoseconds.

Output Timing

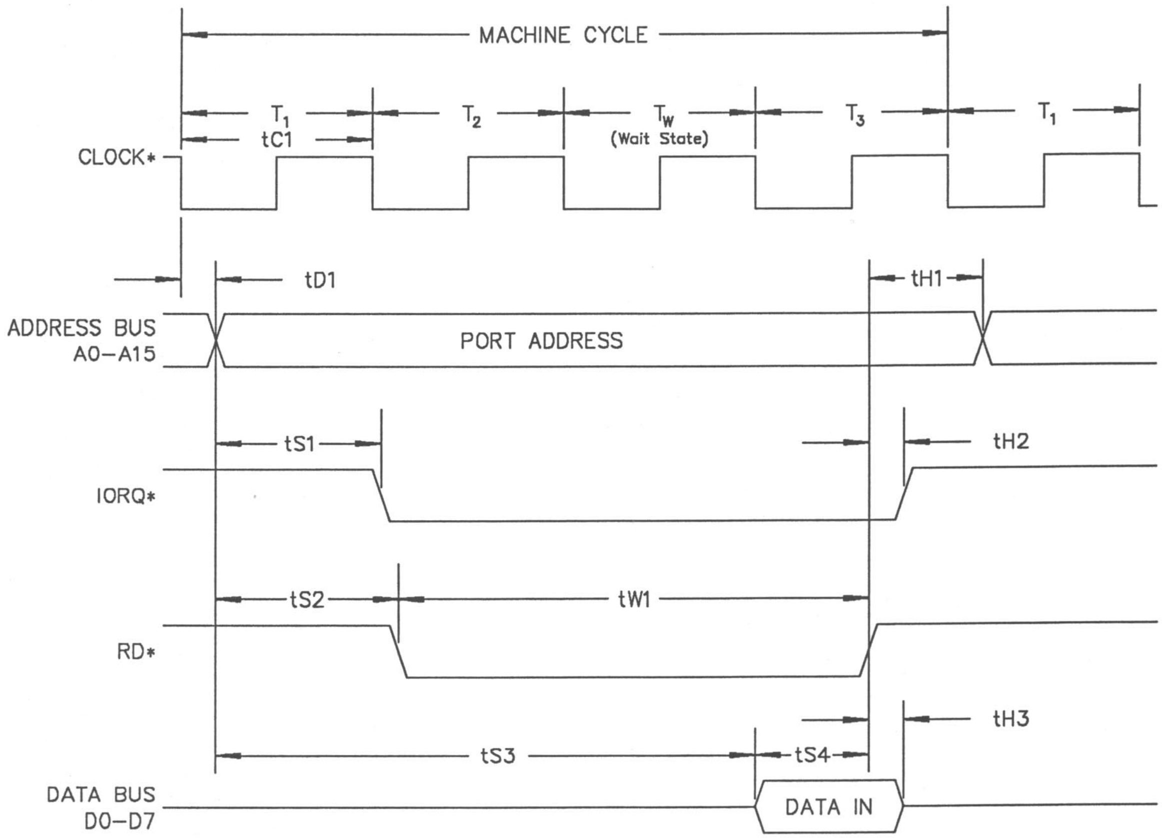


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tS1	Address setup before IORQ* active	300		160		90	
tS2	Address setup before WR* active	310		185		115	
tS3	Address setup before DATA valid	245		130		85	
tS4	Data setup before WR* inactive	1040		650		405	
tH1	Address hold time after WR* inactive	125		45		15	
tH2	IORQ* hold time after WR* inactive	0		0		0	
tH3	Data hold time after WR* inactive	0		0		0	
tW1	WR* pulse width	985		605		250	

Output Timing

All times given in nanoseconds.

Input Timing

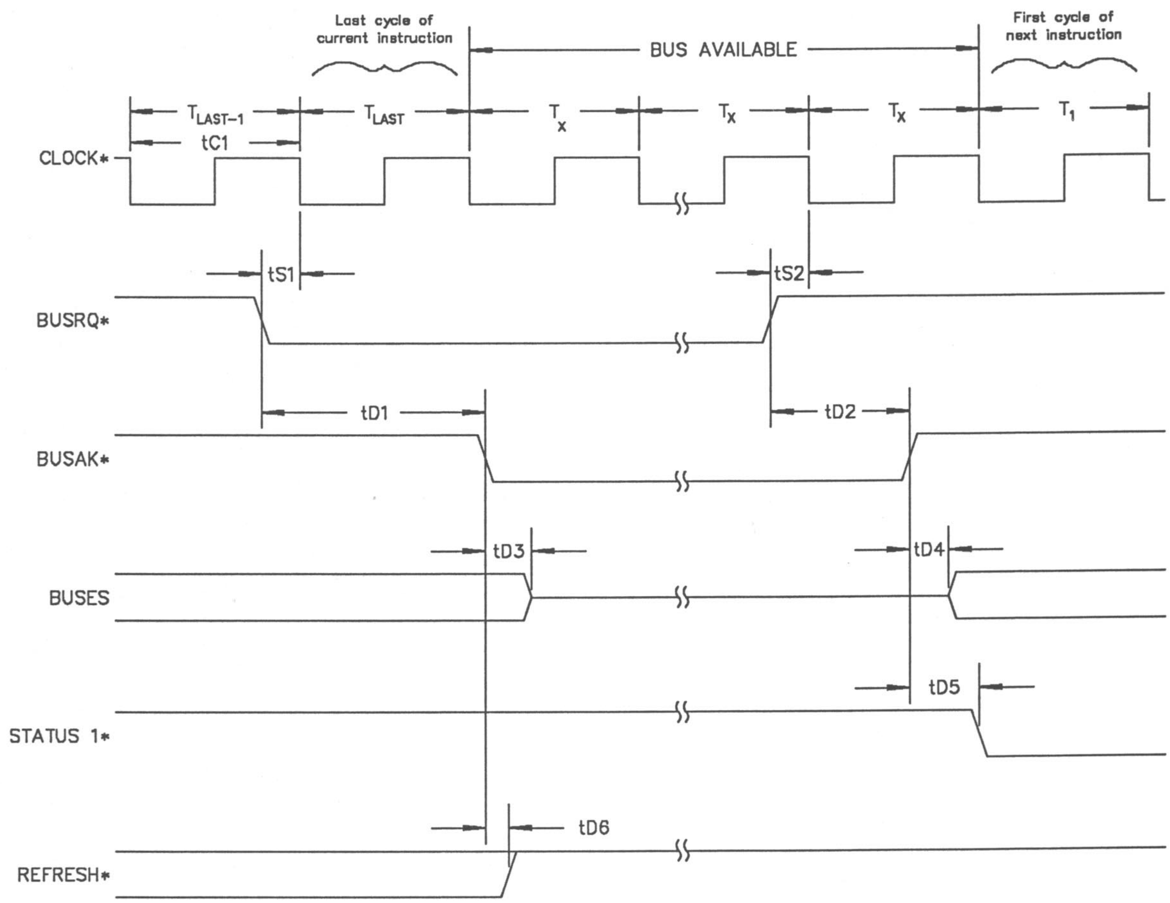


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tS1	Address setup before IORQ* active	300		160		90	
tS2	Address setup before RD* active	330		200		125	
tS3	Address setup before DATA valid	1120		650		380	
tS4	Data setup before RD* inactive	170		145		130	
tH1	Address hold time before RD* inactive	125		45		15	
tH2	IORQ* hold time after RD* inactive	0		0		0	
tH3	Data hold time after RD* inactive	0		0		0	
tW1	RD* pulse width	970		590		375	

Input Timing

All times given in nanoseconds.

Bus Request Timing

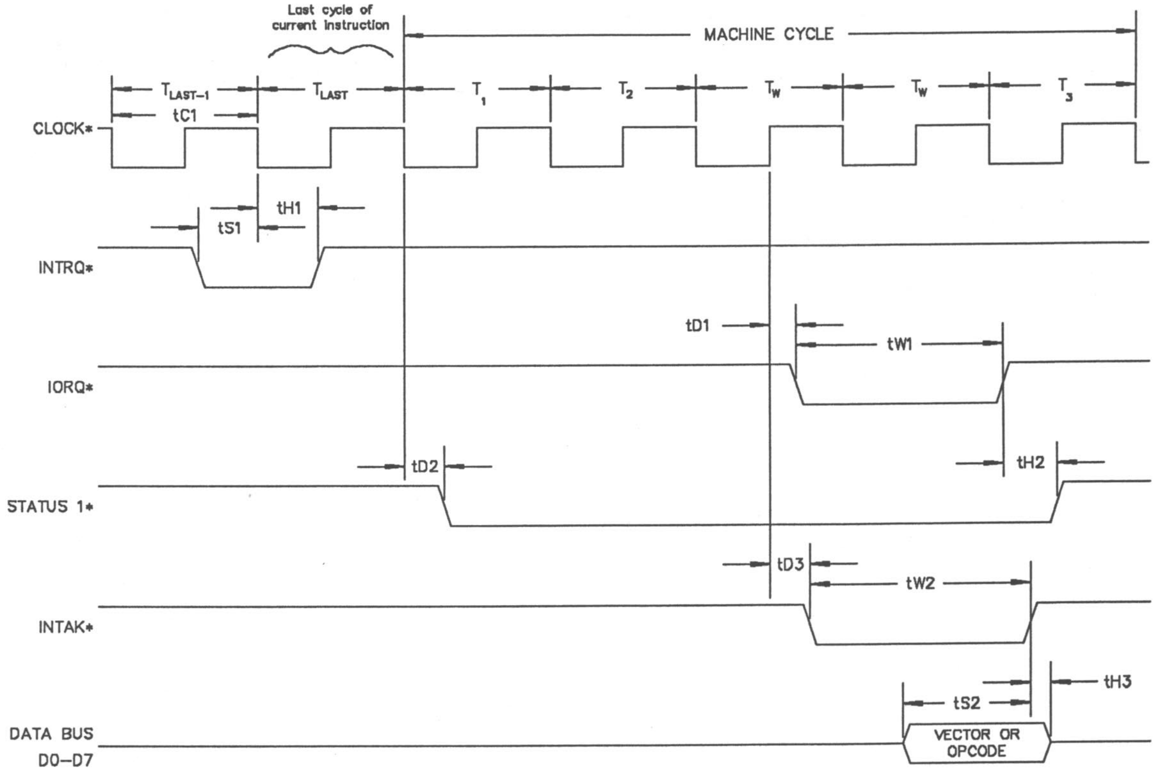


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	BUSAK* delay from BUSRQ* active		655		455		350
tD2	BUSAK* inactive delay from BUSRQ* inactive		455		345		270
tD3	Buses delay after BUSAK* active		50		50		50
tD4	Buses delay after BUSAK* inactive		270		190		135
tD5	STATUS 1* delay after BUSAK* inactive		295		205		140
tD6	REFRESH* delay after BUSAK* active		75		65		55
tS1	BUSRQ* active setup before last time state	100		70		70	
tS2	BUSRQ* inactive setup before last time state	100		70		70	

Bus Request Timing

All times given in nanoseconds.

Interrupt Request Timing

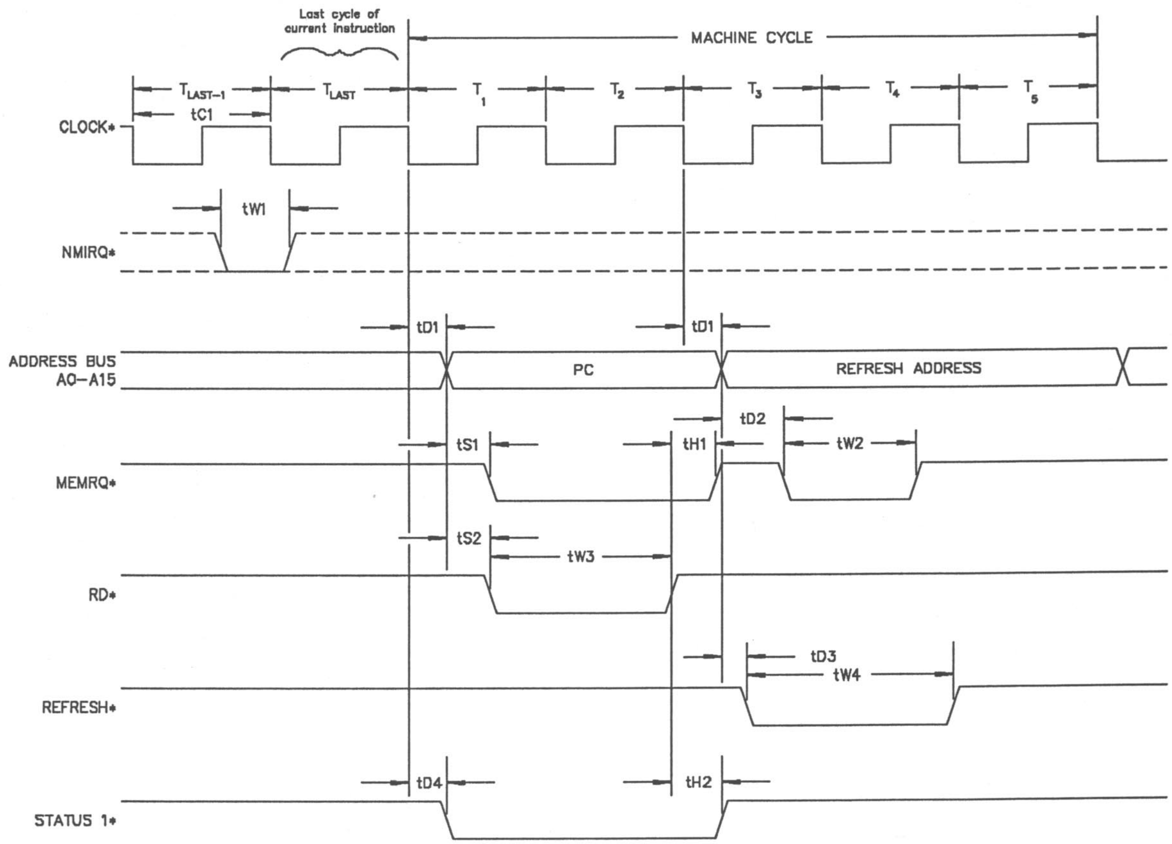


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	IORQ* delay from CLOCK*		130		105		90
tD2	STATUS 1* delay from CLOCK*		150		120		100
tD3	INTAK* delay from CLOCK*		165		140		125
tS1	INTRQ* setup before last time state	120		120		110	
tS2	Data setup before INTAK* inactive	115		85		65	
tH1	INTRQ* hold time after last time state	0		0		0	
tH2	STATUS 1* hold time after IORQ*	10		0		0	
tH3	Data hold time after INTAK* inactive	0		0		0	
tW1	IORQ* pulse width	550		340		205	
tW2	INTAK* pulse width	530		320		190	

Interrupt Request Timing

All times given in nanoseconds.

Non Maskable Interrupt Request Timing

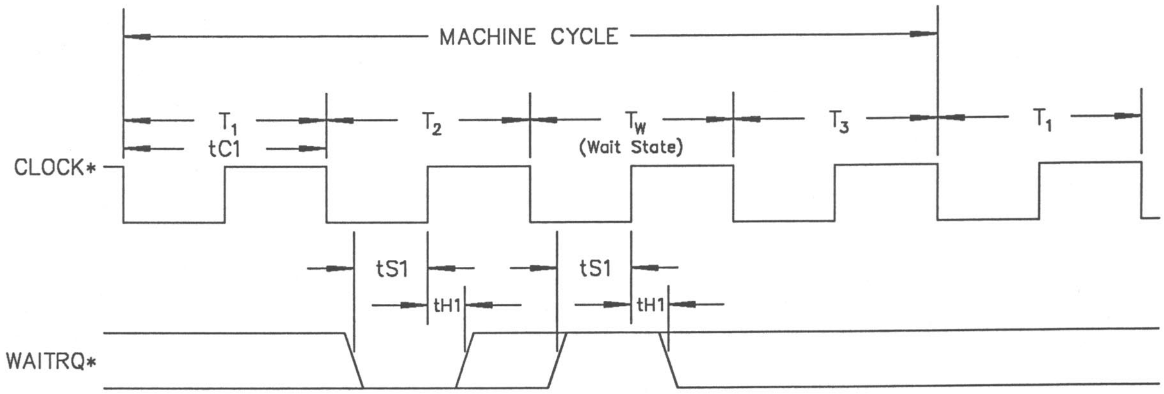


Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tD1	Address delay from CLOCK*		165		130		110
tD2	MEMRQ* delay from Refresh Address valid		155		115		65
tD3	REFRESH delay from Refresh Address valid		55		40		40
tD4	STATUS 1* delay from CLOCK*		150		120		100
tS1	Address setup before MEMRQ* active	90		30		15	
tS2	Address setup before RD* active	150		80		40	
tH1	MEMRQ* hold time after RD* inactive	0		0		0	
tH2	STATUS 1* hold time after RD* inactive	15		0		0	
tW1	NMIRQ* pulse width	60		60		50	
tW2	MEMRQ* pulse width (REFRESH)	335		195		115	
tW3	RD* pulse width	520		310		200	
tW4	REFRESH* pulse width	735		460		295	

Non Maskable Interrupt Request Timing

All times given in nanoseconds.

Wait State Timing



Symbol	Parameter	2.5 MHz MIN	2.5 MHz MAX	4.0 MHz MIN	4.0 MHz MAX	6.0 MHz MIN	6.0 MHz MAX
tC1	Clock cycle time	400		250		165	
tS1	WAITRQ* setup before CLOCK*	110		110		100	
tH1	WAITRQ* hold time after CLOCK*	0		0		0	

Wait State Timing

All times given in nanoseconds.